

Husk/Petra UMA/Muxless Schematics Document Ivy Bridge Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

DIS I/B Touch

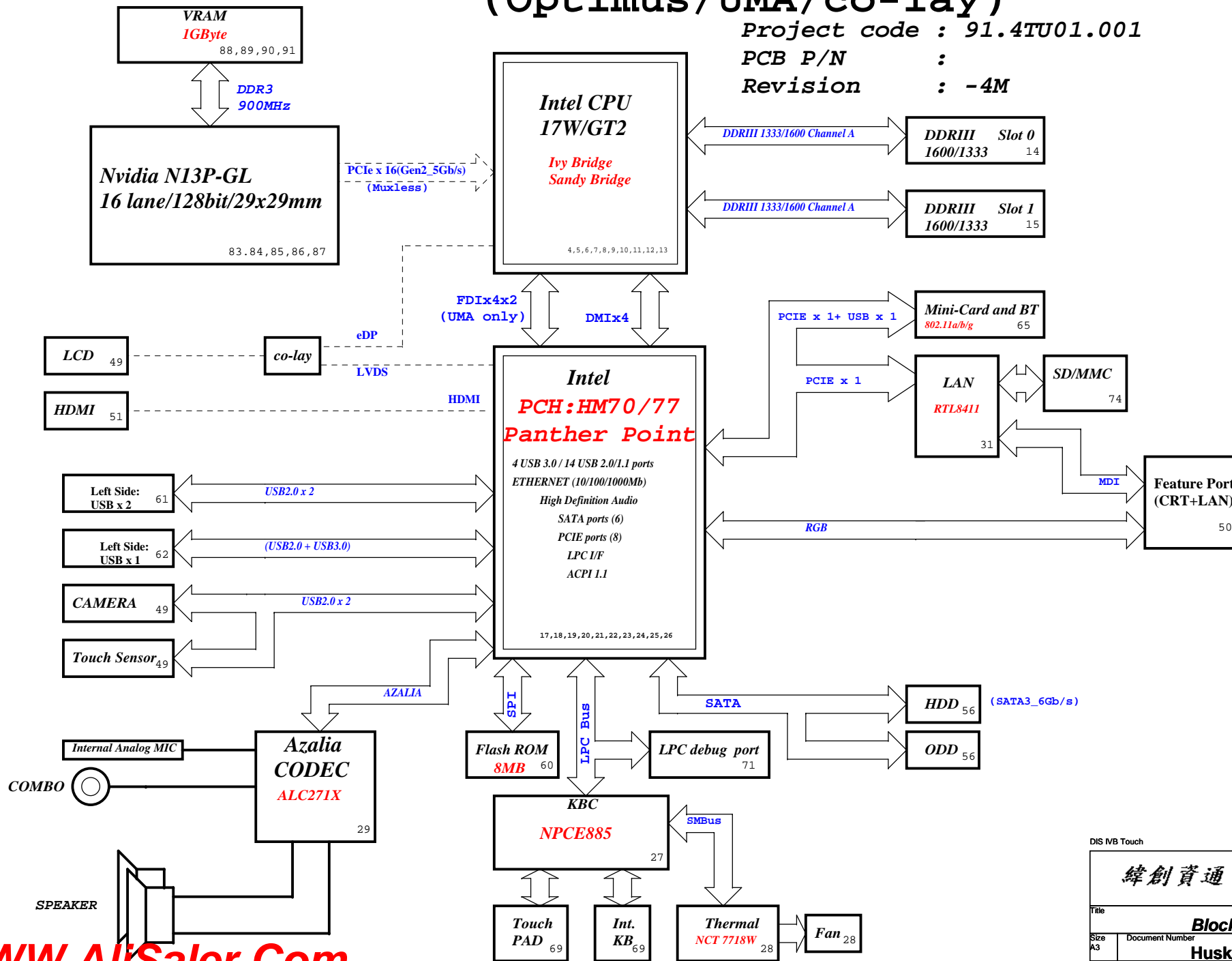
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Title			
Cover Page			
Size A3	Document Number Husk/Petra	Rev -4M	
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Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001

PCB P/N :

Revision : -4M



CHARGER	
BQ24727	40
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT8223MGQW	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
CPU DC/DC	
ISL95836HRTZ	42~43
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
ISL95836HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218DSCR	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207LGQW	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
LDO	
RT9025-25ZSP	47
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
LDO	
G978	48
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0
VGA	
ISL62882CHRTZ	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0
PCB LAYER	
L1:Top L4:Signal L2:VCC L5:GND L3:Signal L6:Bottom	

DIS I/B Touch

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Block Diagram		
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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

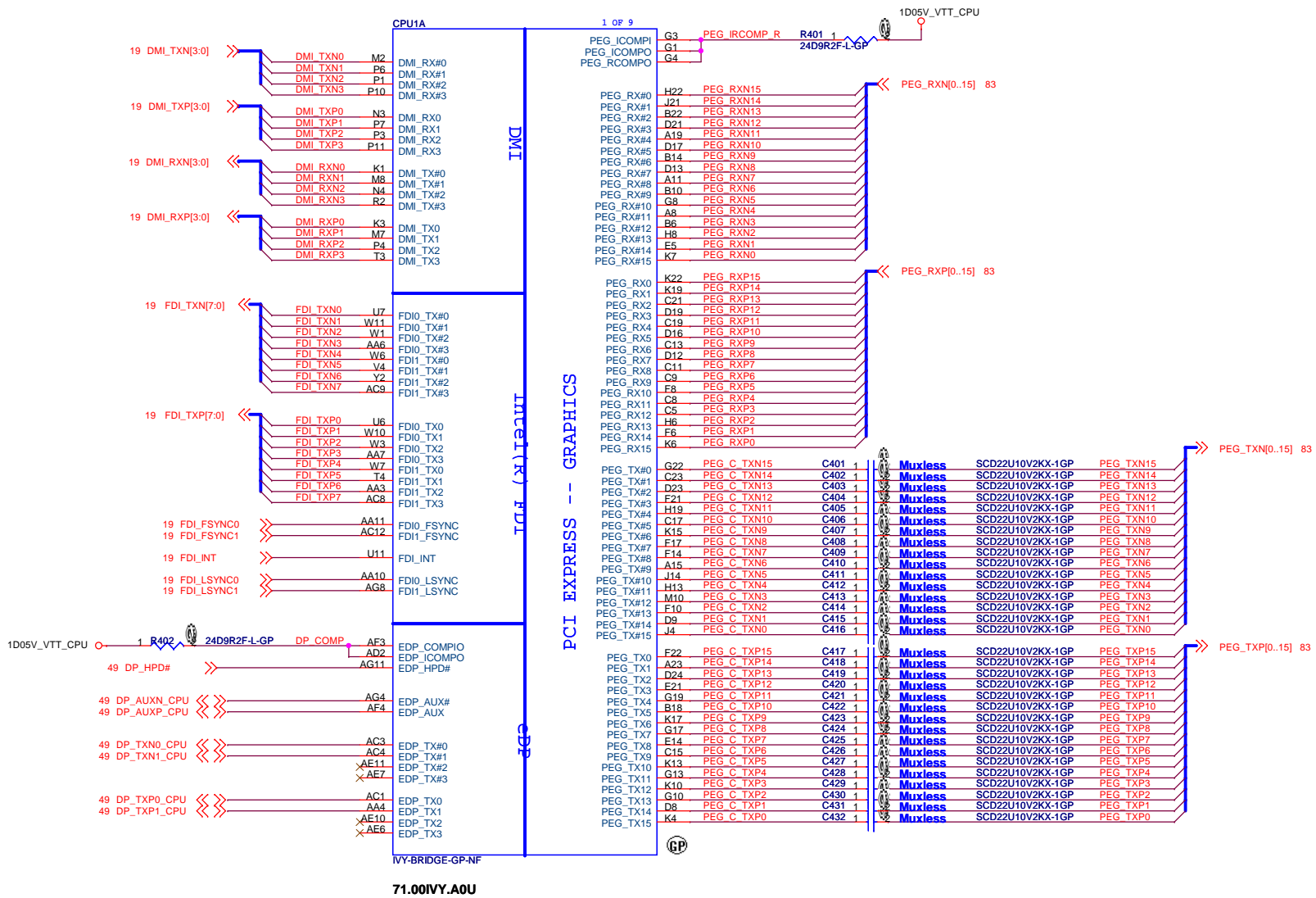
I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB	
Device			Address	Hex Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMM(A) (SPP) SO-DIMM(B) (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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File			
Table of Content			
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SSID = CPU

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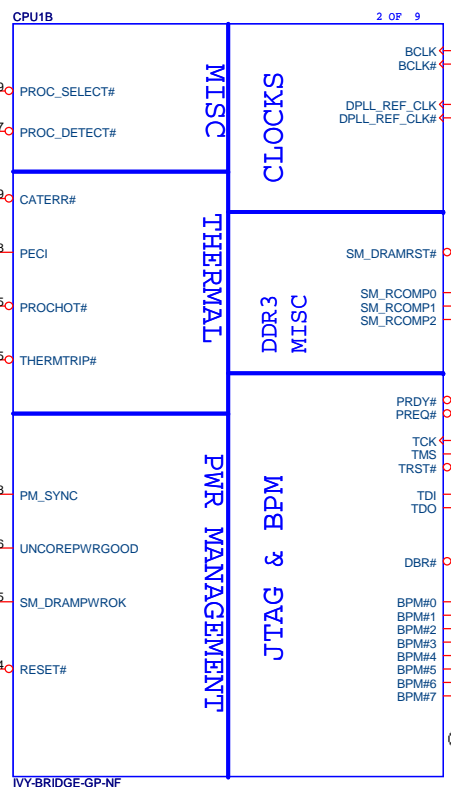
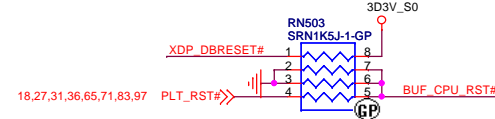
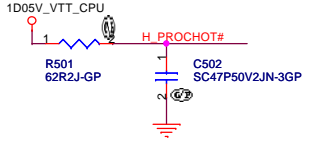
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Title: **CPU (PCIe/DMI/FDI)**

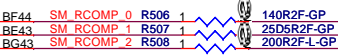
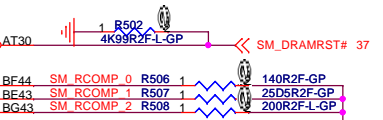
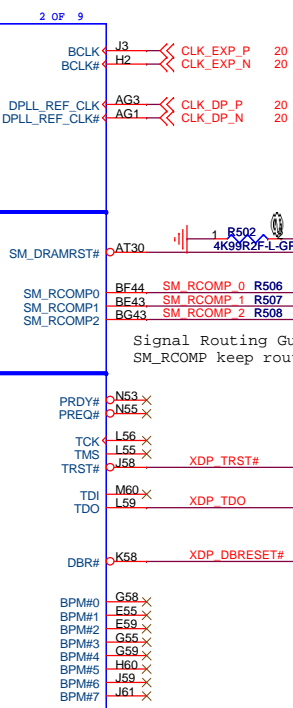
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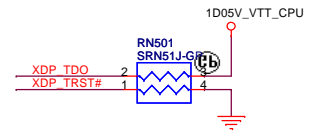
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71.00IVY.A0U



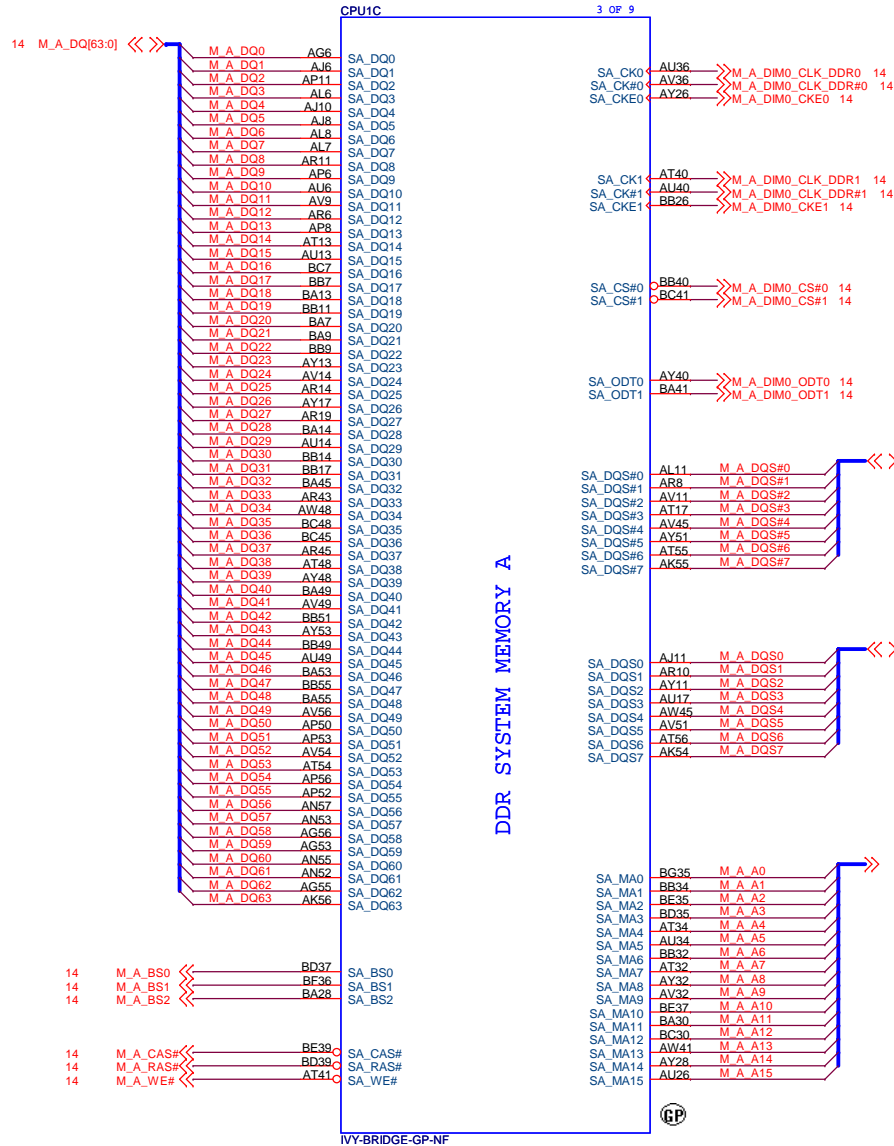
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



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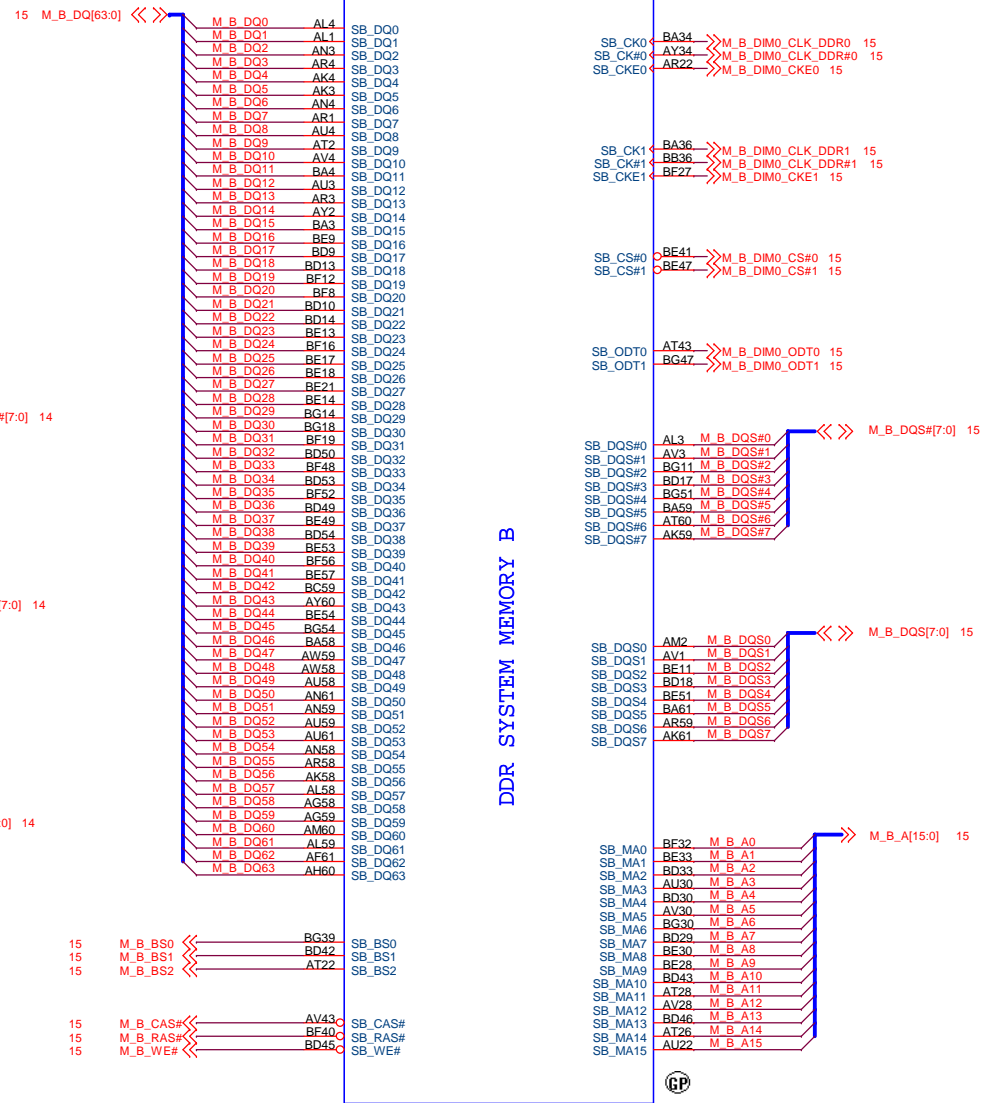
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Custom			
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IVY-BRIDGE-GP-NF

71.00IVY.A0U



IVY-BRIDGE-GP-NF

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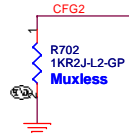
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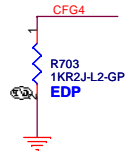
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SSID = CPU

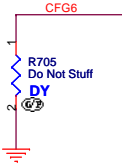
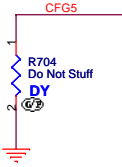
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



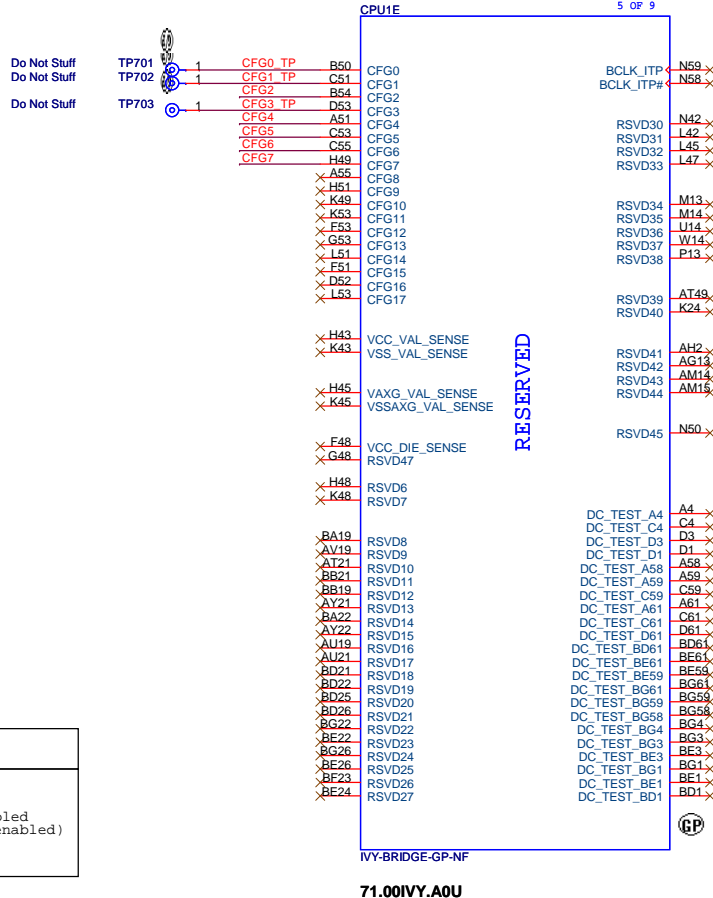
Enabl EDP function	
CFG4	1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

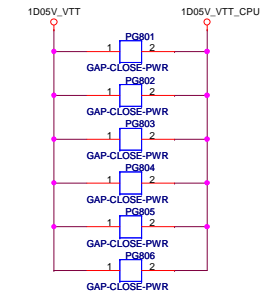
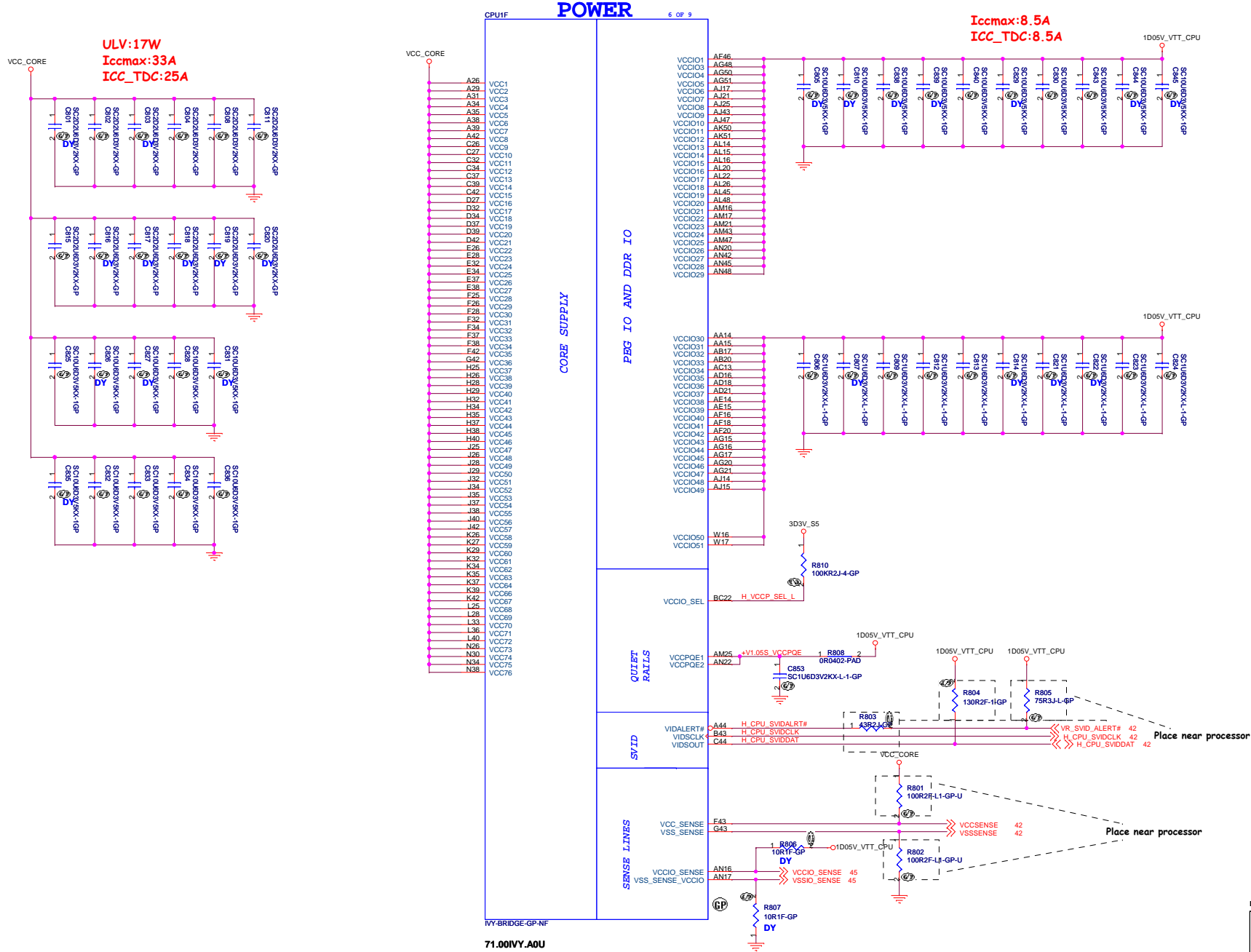


PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



71.00IVY.A0U

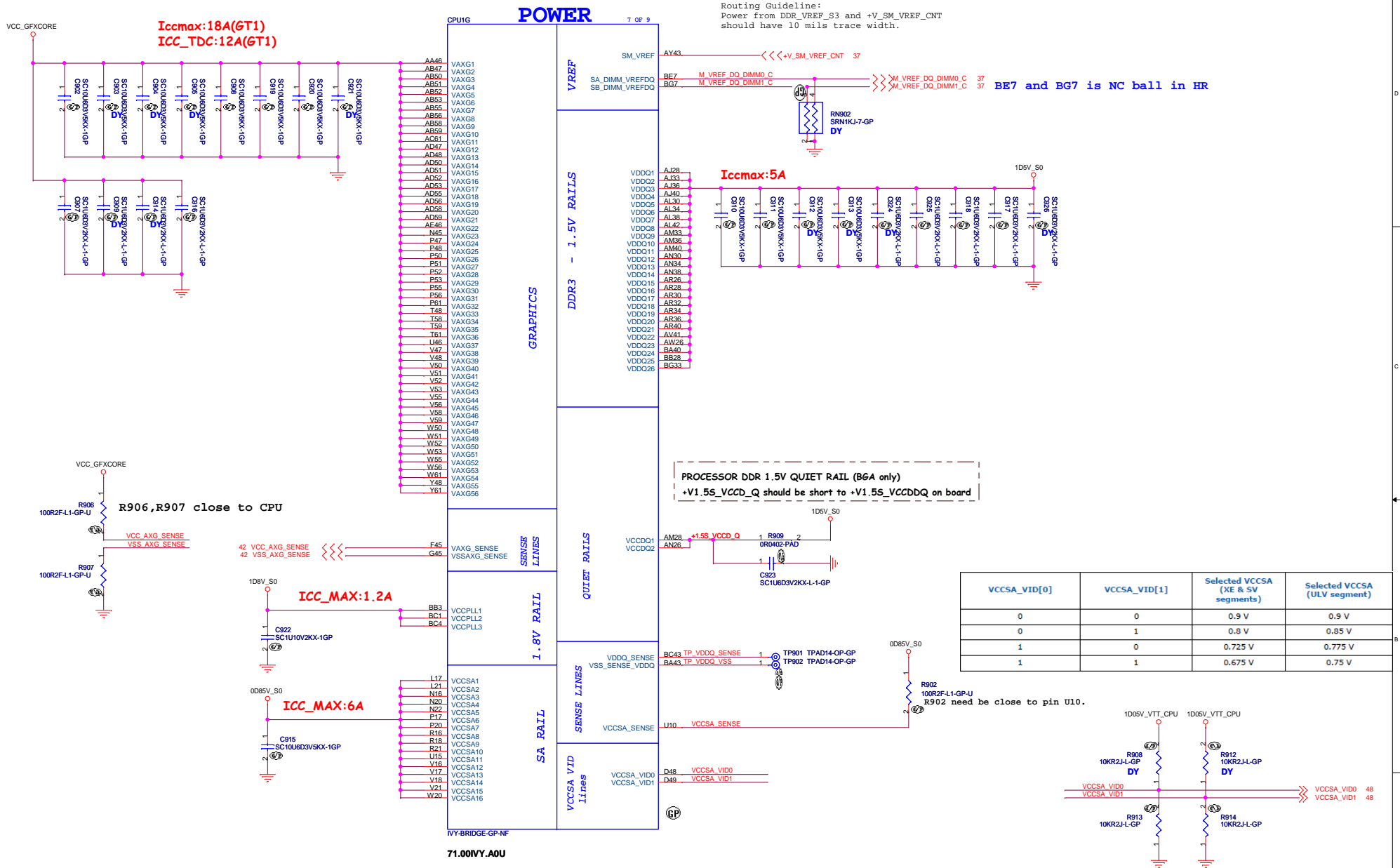
SSID = CPU



DIS MB Touch

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Title			
CPU (VCC CORE)			
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Title

CPU (VCC GFXCORE)

Size

Document Number

Husk/Petra

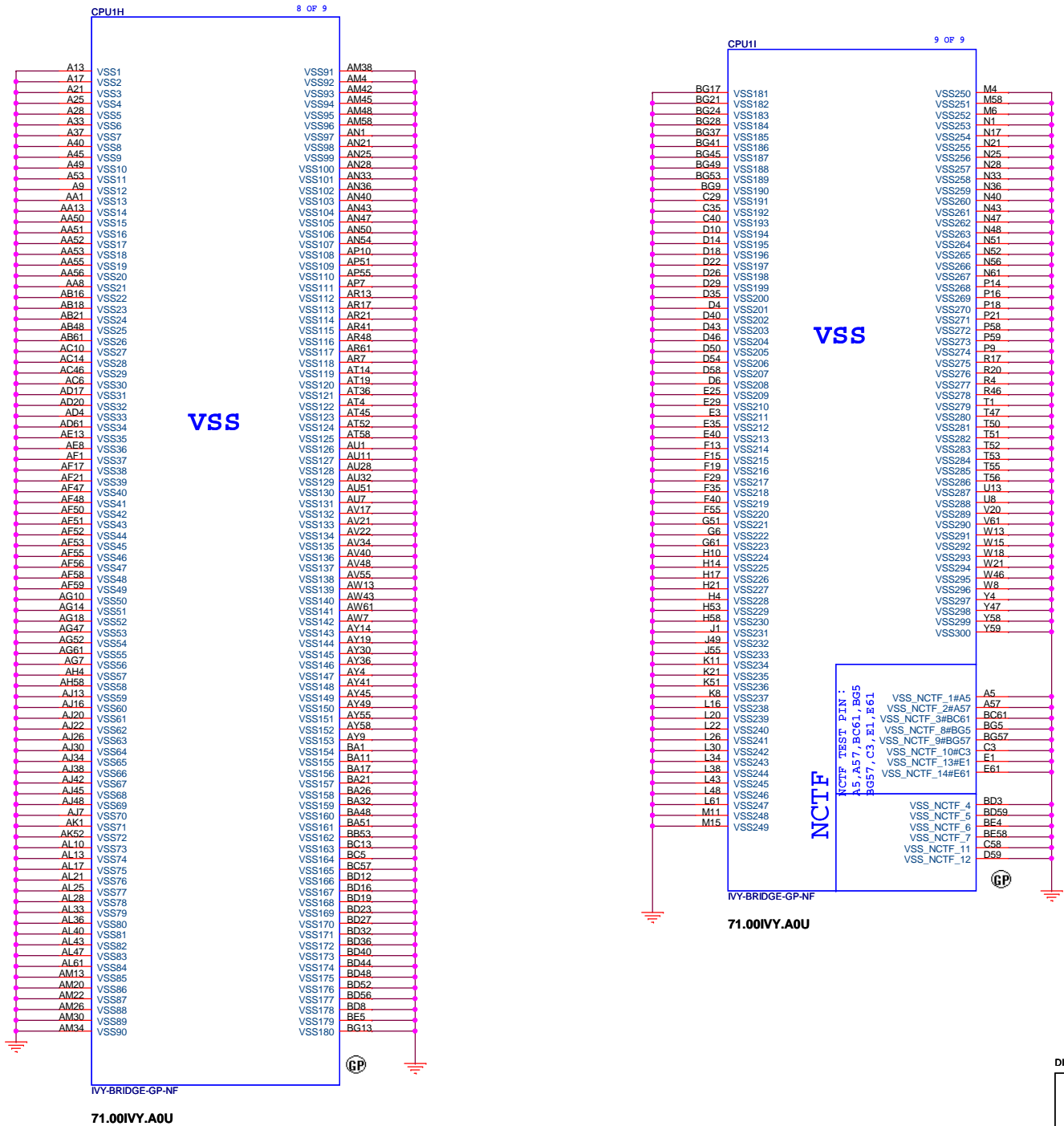
Rev

-4M

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SSID = CPU



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Title

CPU (VSS)

Size

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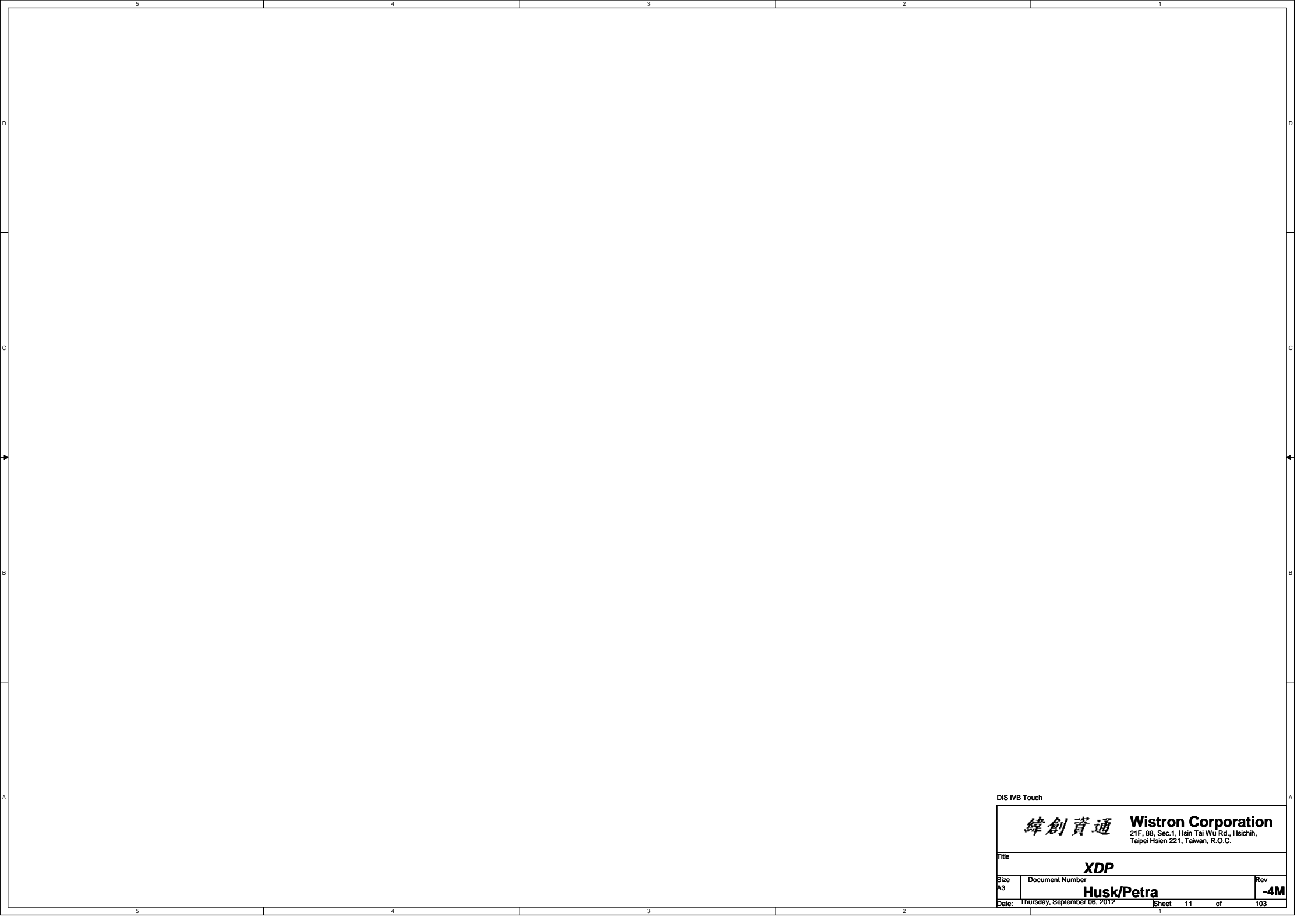
Husk/Petra

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D

D

C

C

B

B

A

A

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Size	Document Number	Rev
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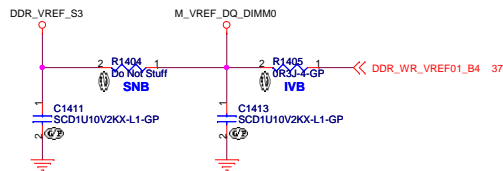
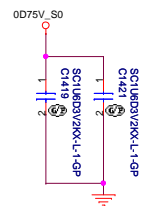
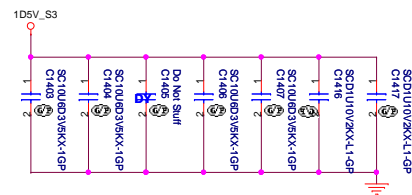
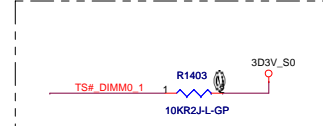
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—<> M_A_A[15:0] 6



Tracew should be at least 20 mils wide

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[illegible]**DDR3-SODIMM1**

Size

Document Number

Husk/PetraRev
-4M

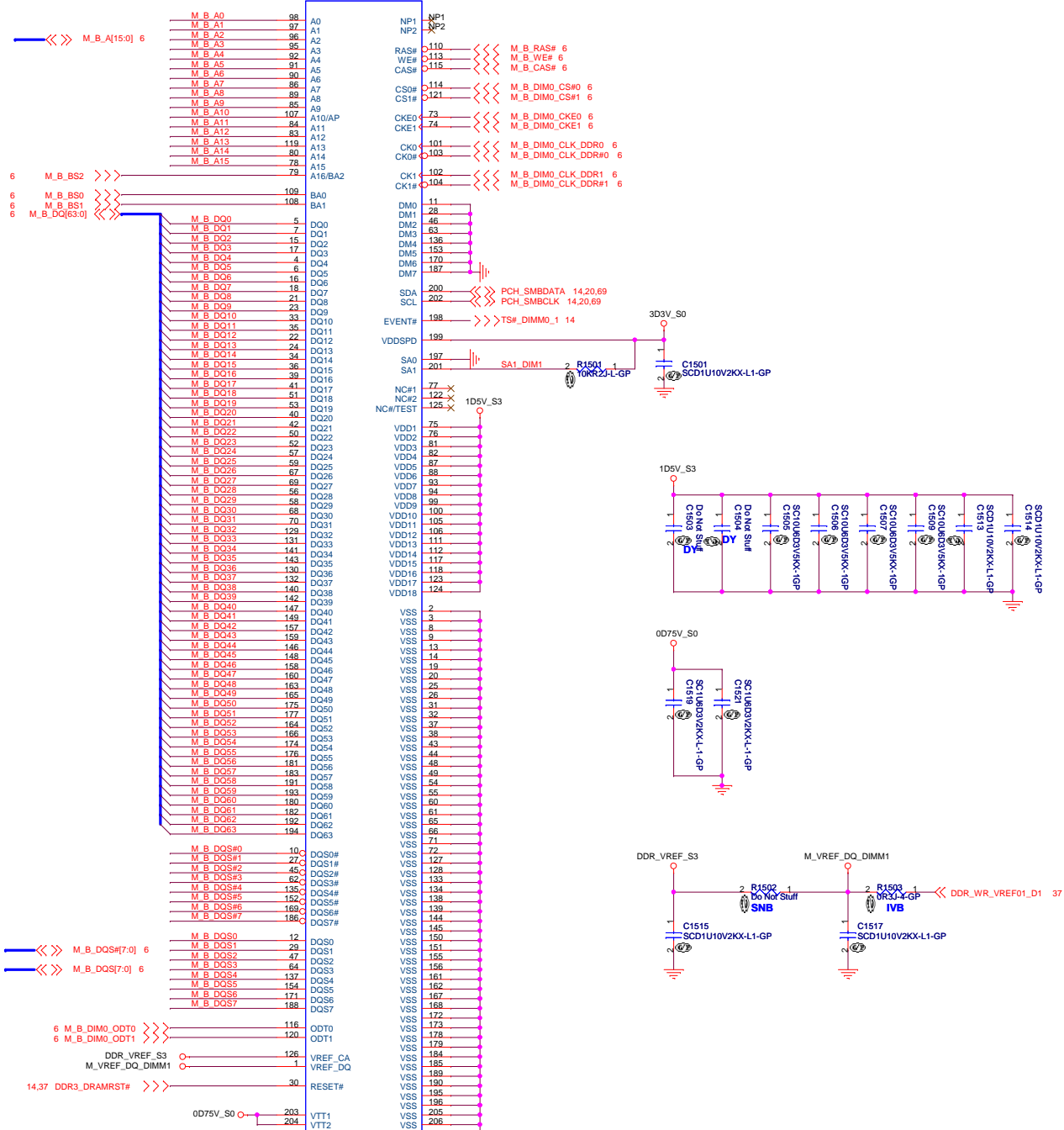
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SSID = MEMORY



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Title

DDR3-SODIMM2

Size

Document Number	
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Husk/Petra

Rev	-4M
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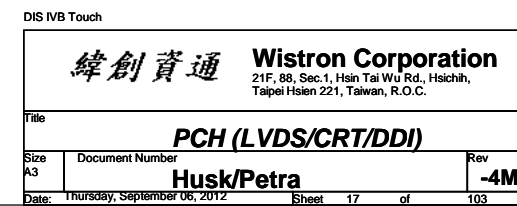
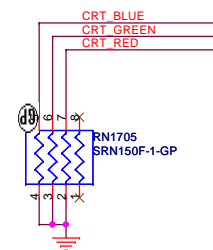
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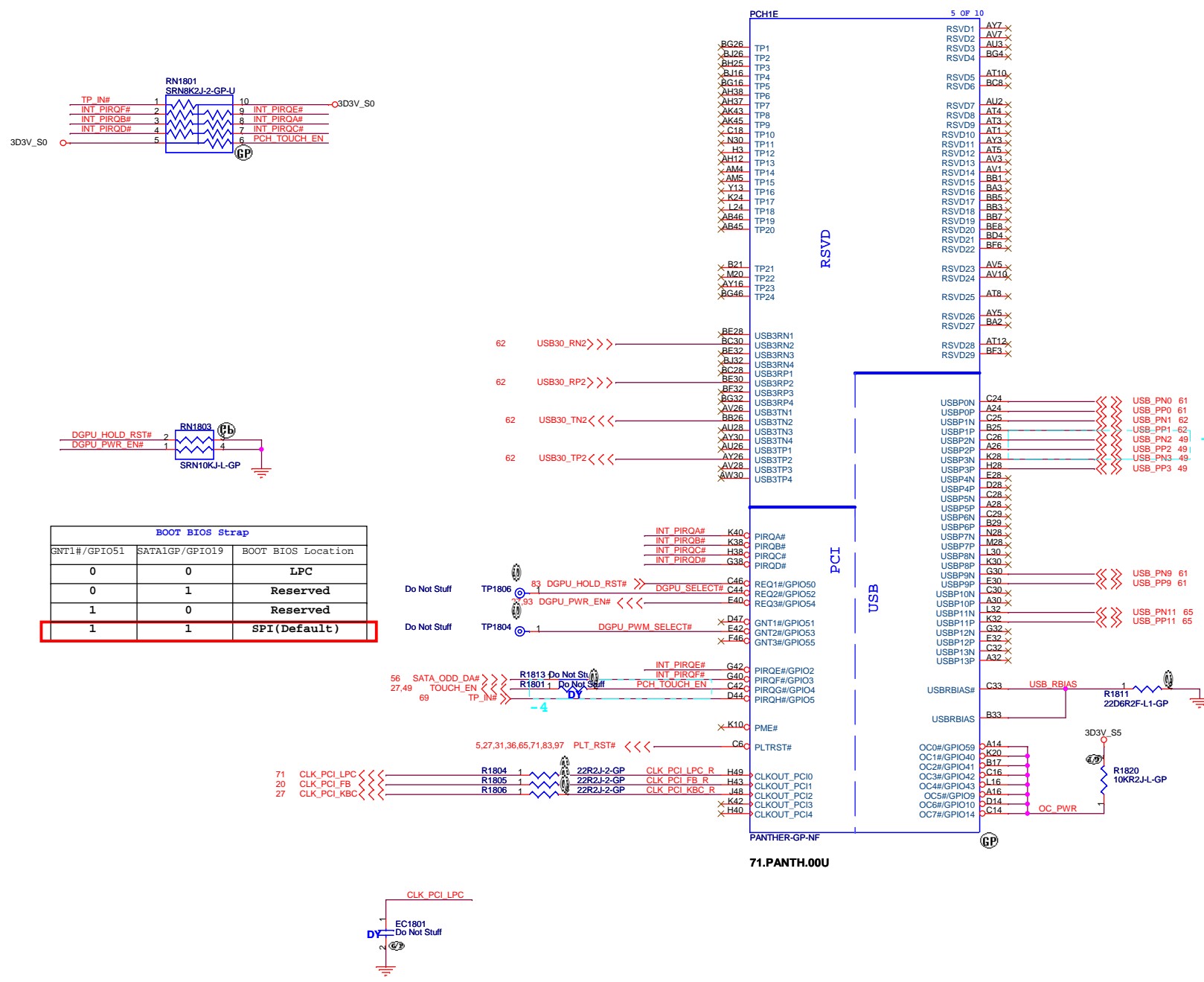
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SSID = PCH

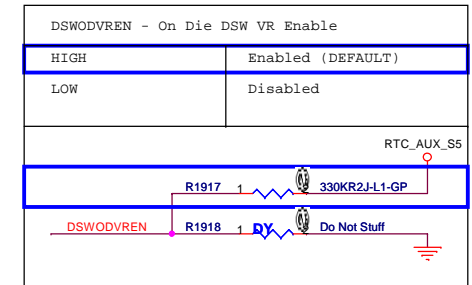


BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	Touch panel
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.



3D3V_S5

RN1901
SRN10KJ-6-GP

8 1 BATLOW#

7 2 PM R#

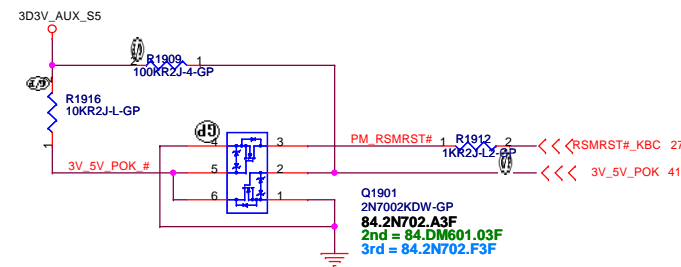
6 3 AC PRESENT

5 4 SUS_PWR_ACK R

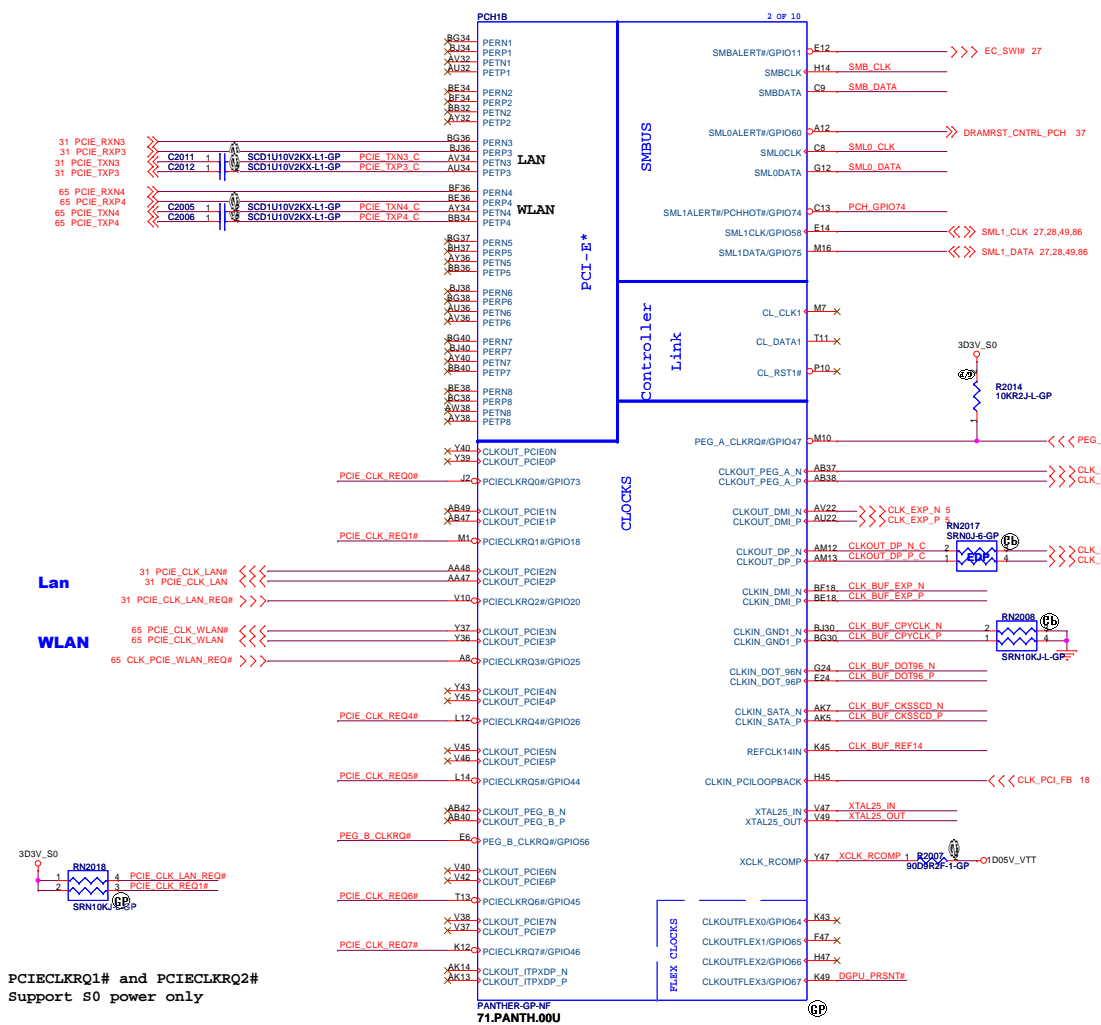
PCIE_WAKE#

SUS_PWR_ACK#

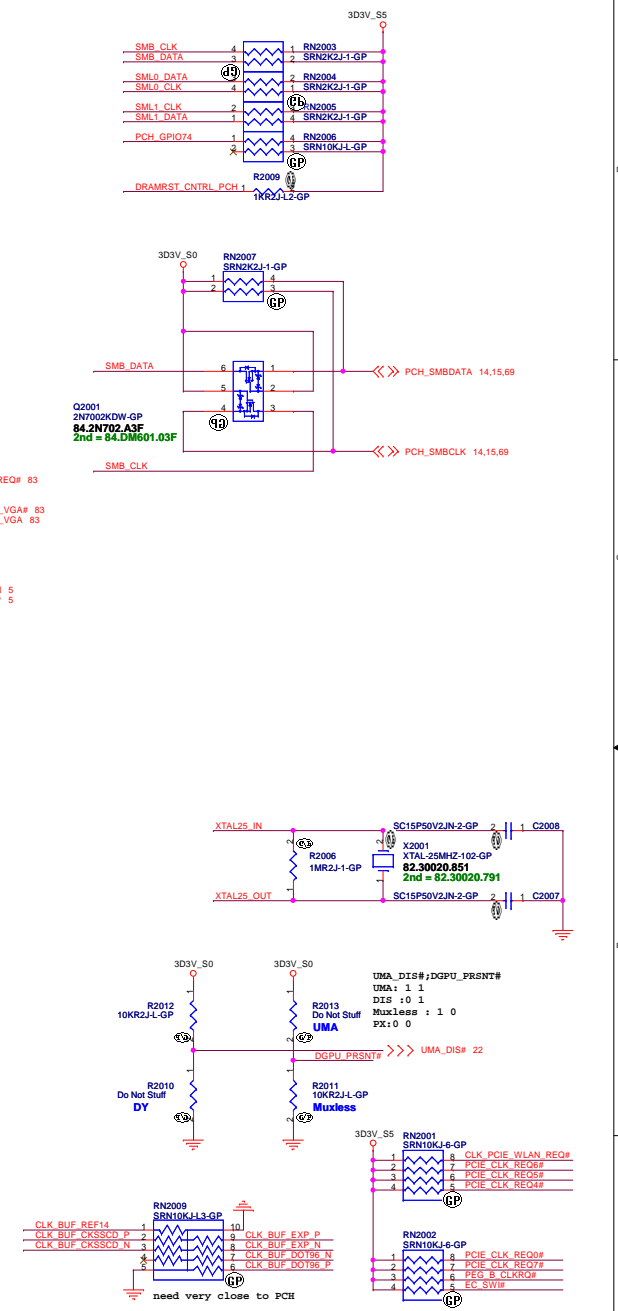
PM RSMRST#



SSID = PCH



PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only



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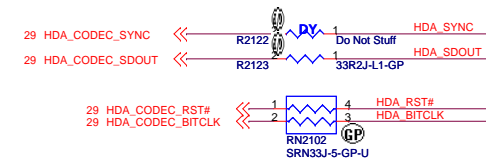
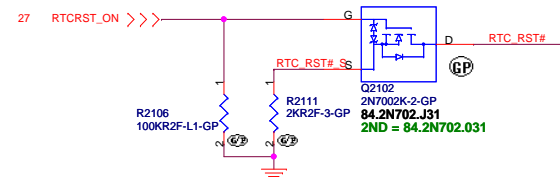
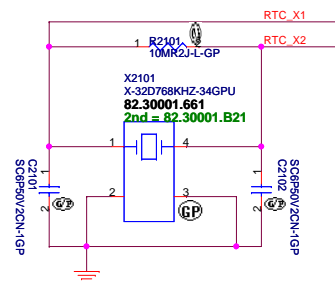
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Taipai Hsien 221, Taiwan, R.O.C.

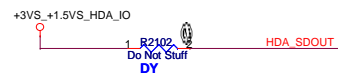
Title: PCH (PCI-E/SMBUS/CLOCK/KL)
Size: Document Number
Customer: Husk/Petra
Date: Thursday, September 06, 2012
Sheet: 20 of 103

Rev: -4M

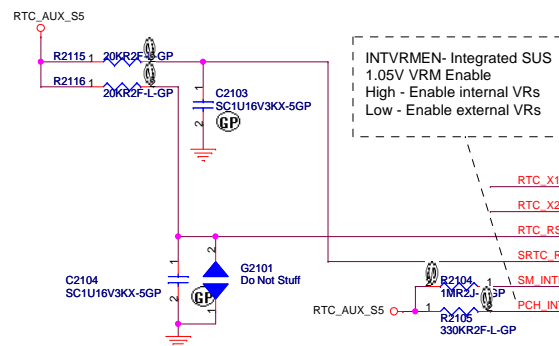
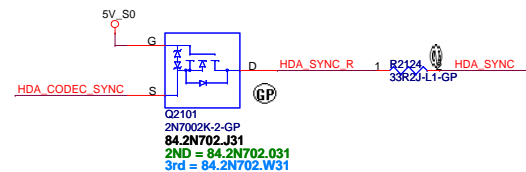
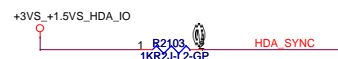
SSID = PCH



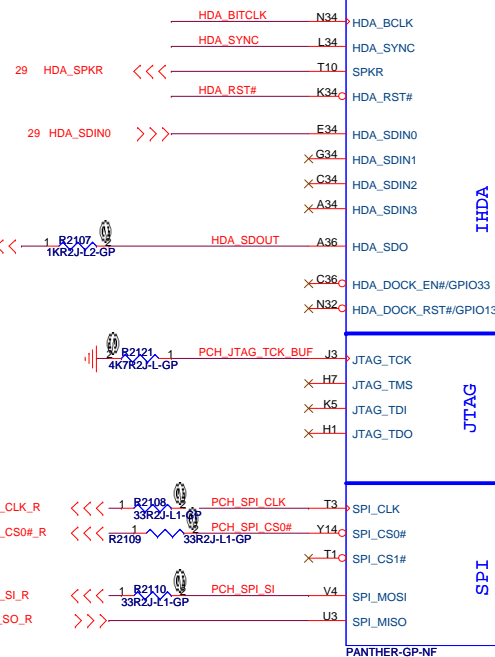
Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Enable



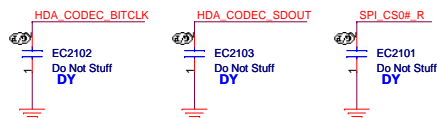
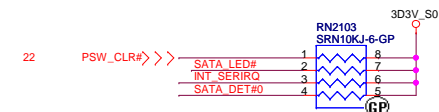
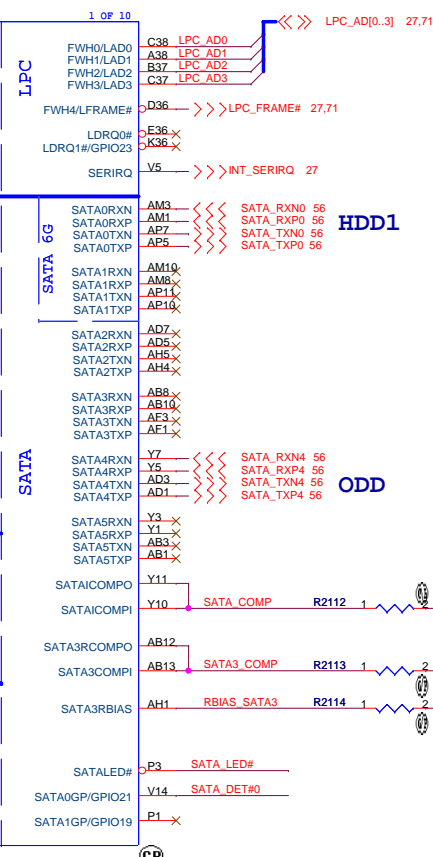
PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



RTC Reset



71.PANTH.00U



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

DIS IVB Touch

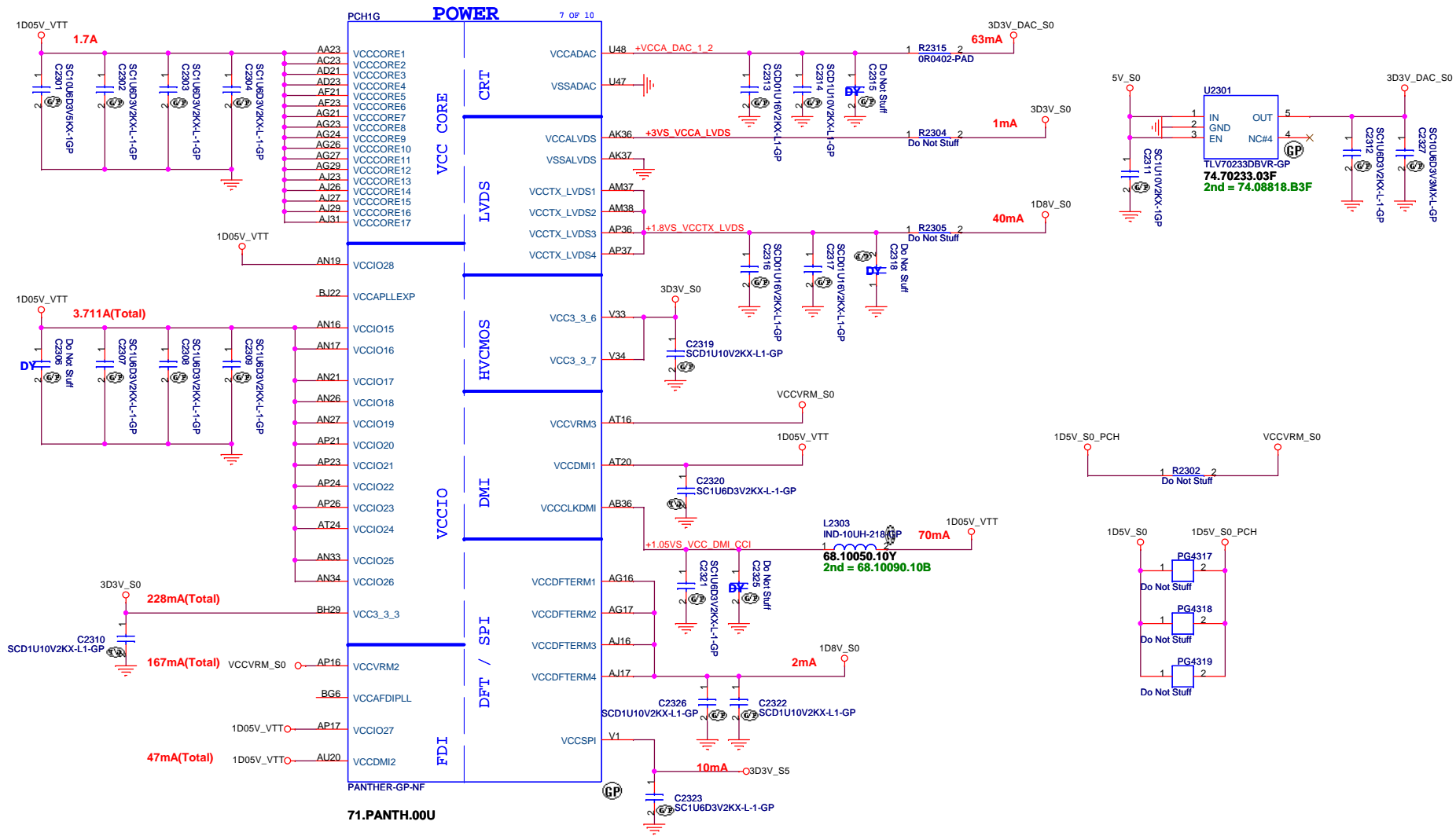
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number	Rev	
Custom	Husk/Petra	-4-	
Date:	Thursday, September 06, 2012	Sheet	21 of 103



SSID = PCH



DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (POWER1)

Size
A3

Document Number	
-----------------	--

Husk/Petra

Rev

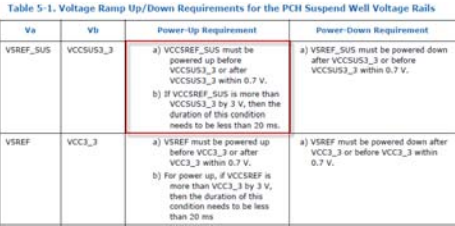
	-4M
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Date: Thursday, September 06, 2012

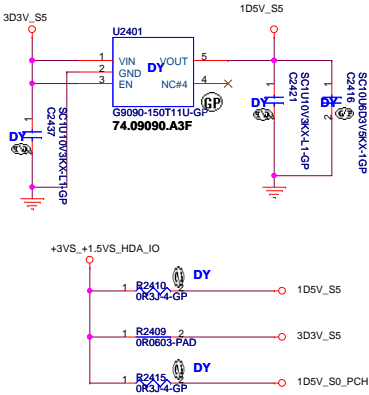
Sheet	23	of	103
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[illegible]

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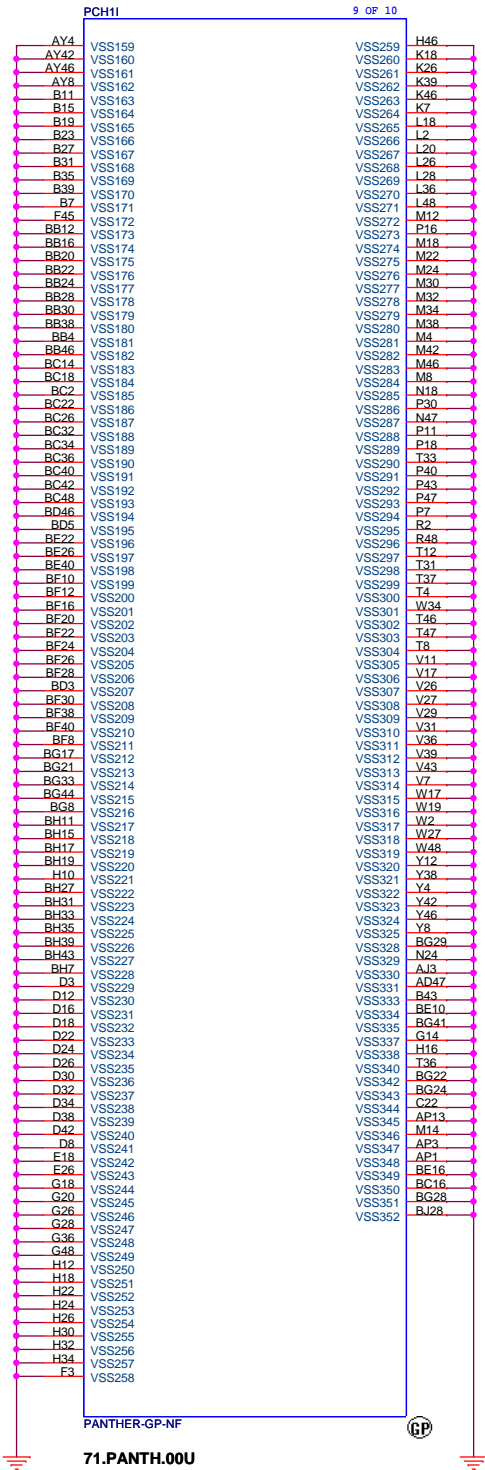
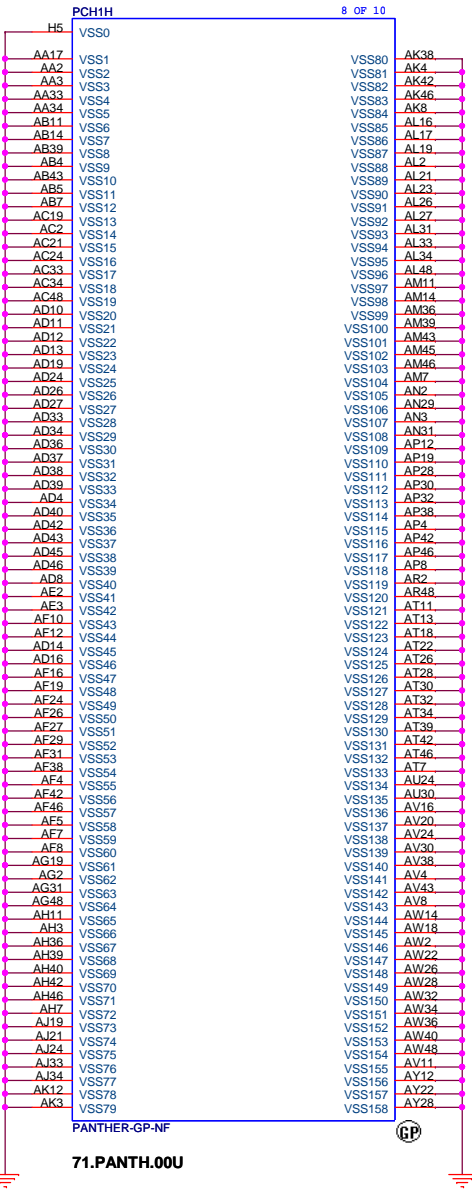


VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



DIS IVB Touch

SSID = PCH



DIS IVB Touch

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Title **PCH (VSS)**

Size A3 Document Number **Husk/Petra** Rev **-4M**

Date: Thursday, September 06, 2012 Sheet 25 of 103

DIS IVB Touch

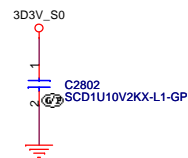
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Clock(colay)</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 26 of 103



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.40V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V

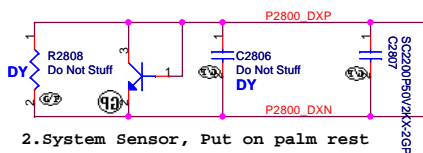
SSID = Thermal

Thermal sensor NCT 7718W

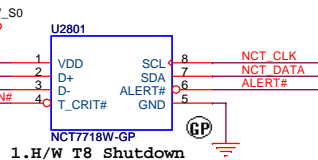


Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

Q2801
PMBS3904-1-GP
84.03904.L06



2.System Sensor, Put on palm rest



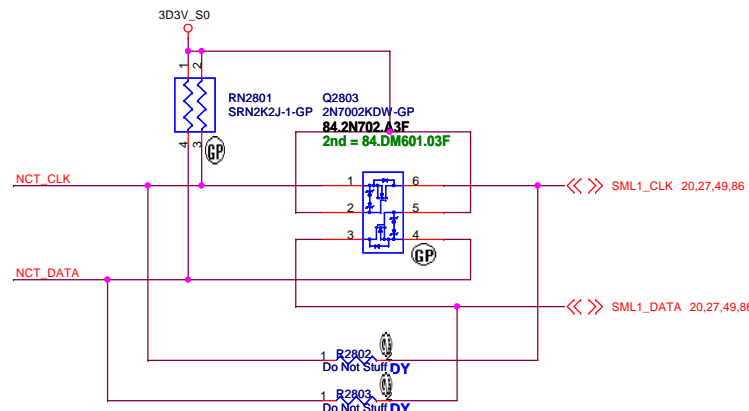
1.H/W T8 Shutdown

ALERT# /T CRIT#
Pull-up Resistor

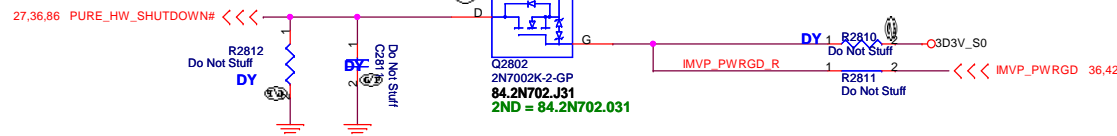
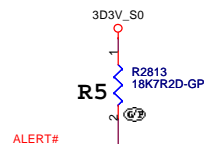
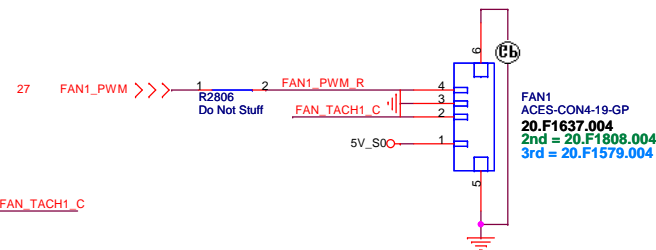
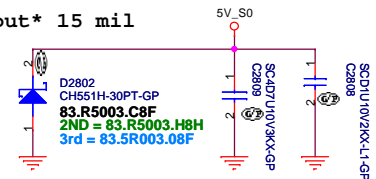
	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	2Kohm	77°C	87°C	97°C	107°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

SB T8=85 degree



Layout 15 mil



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Title			
Thermal NCT7718			
Size	Document Number		Rev
Custom	Husk/Petra		-4M
Date:	Thursday, September 06, 2012	Sheet 28 of	103



D

1

C

C

B

E

A

A

DIS IVB Touch

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Title

Audio AMP

Size	A3
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Document Number

Husk/Petra

Rev

-4M

Date: Thursday, September 06, 2012

Sheet 30 of 103

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Title			
LAN(RTL8411)			
Size Custom	Document Number		Rev
	Husk/Petra		-4M
Date:	Thursday, September 06, 2012	Sheet 31 of 103	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

DIS IVB Touch

<div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>	
Title	
RTS5159 (CARD READER)	
Size	Document Number
Custom	Husk/Petra
Date	Thursday, September 06, 2012
Rev	-4M
Sheet	32 of 103

(Blanking)

DIS IVB Touch

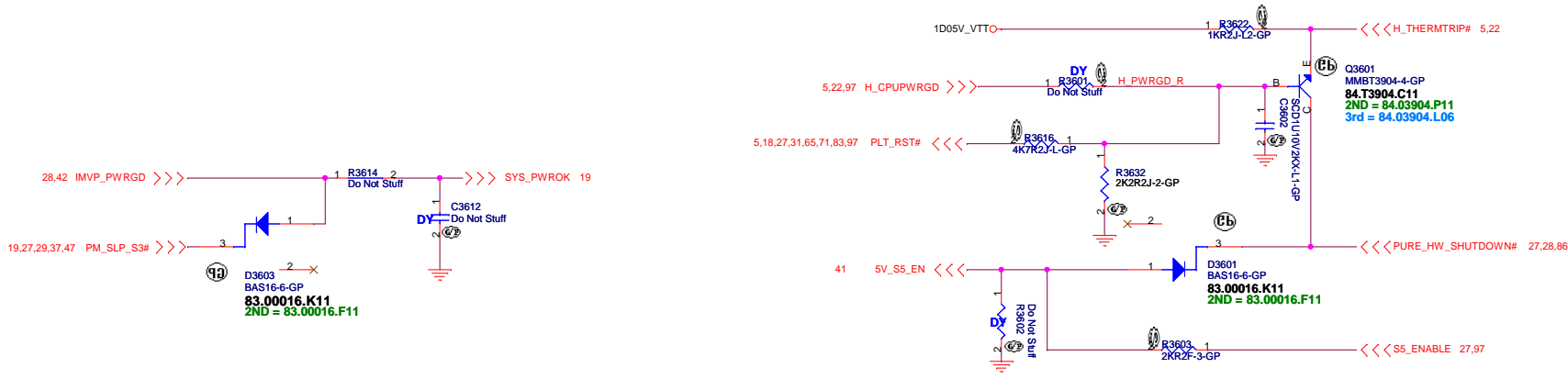
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 33 of 103

(Blanking)

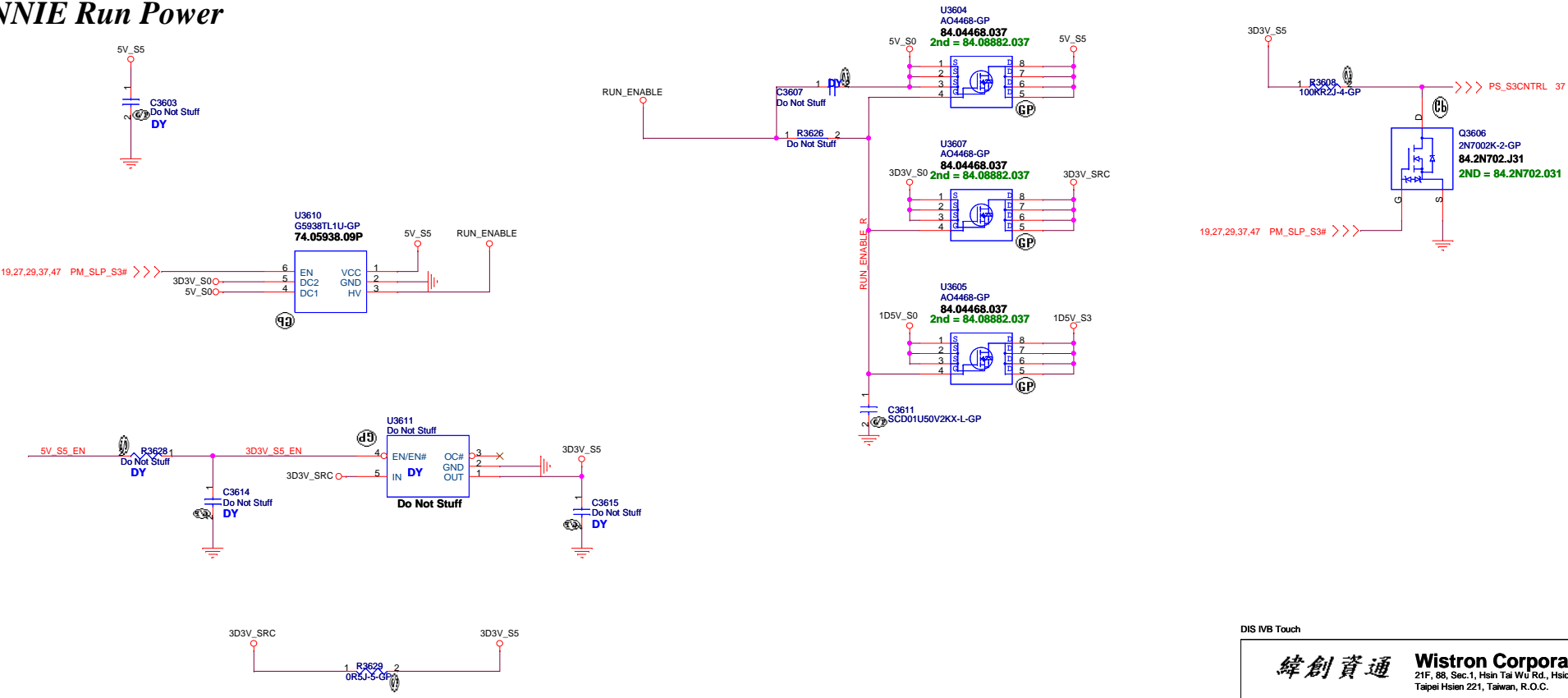
DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 34 of 103

Power Sequence



ANNIE Run Power



DIS IVB Touch

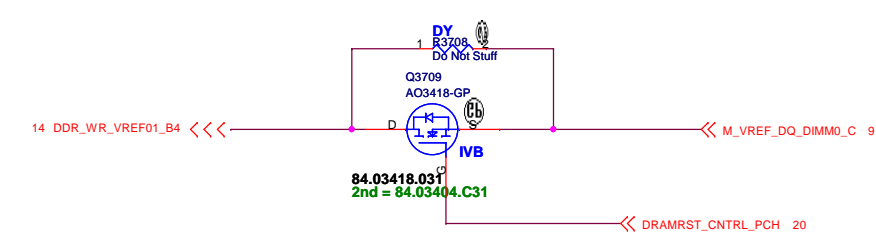
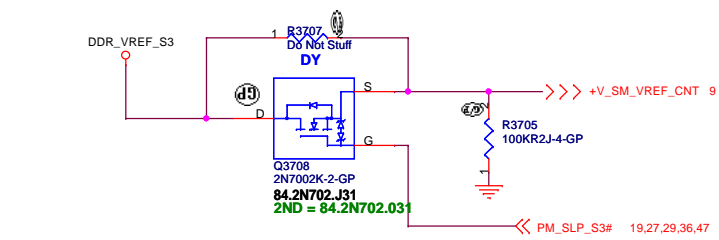
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Power Plane Enable**

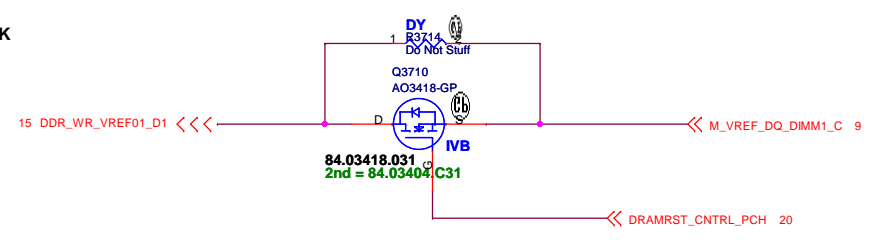
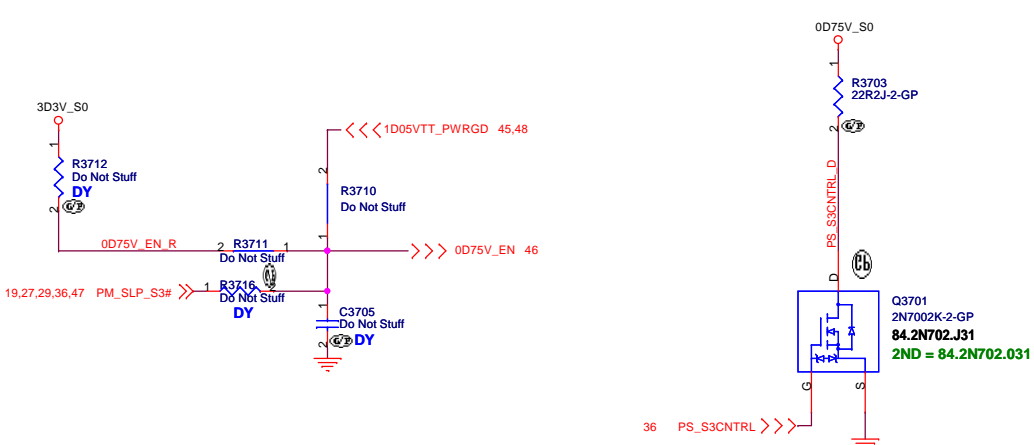
Size Custom Document Number **Husk/Petra** Rev **-4M**

Date: Thursday, September 06, 2012 Sheet 36 of 103

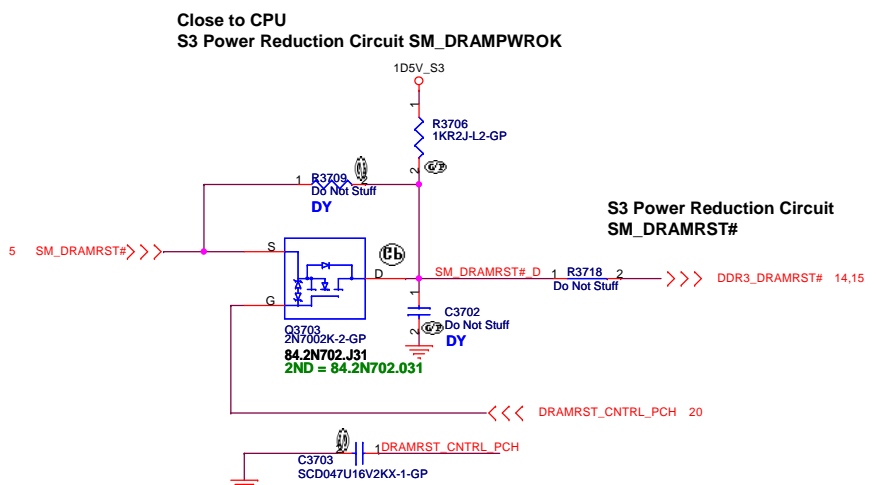
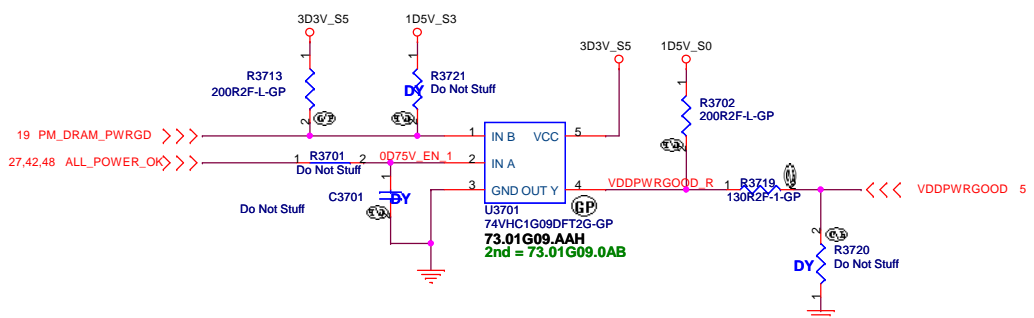
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

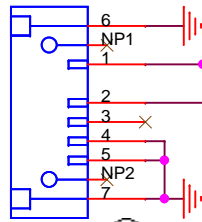


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

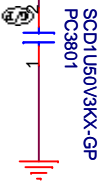


S3 Power Reduction Circuit
SM_DRAMRST#

1Pin=3A



DCIN1
ACES-CON5-27-GP
20.F2182.005
2nd = 20.F2198.005



PC3801
SCD1U50V3KX-GP



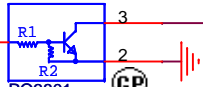
D3801
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG



PC3802
SC1U50V5ZY-1-GP

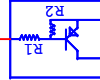
27

AD_OFF >>>



PQ3801
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR_ADJK_EN



PQ3802
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

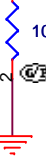
AD_JK



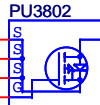
PR3807
200KR2F-L-GP



PC3805
SC1U50V5ZY-1-GP



PR3808
100KR2J-4-GP



PU3802
P1403EV8-GP
84.P1403.B37
2nd = 84.04407.F37
3rd = 84.03005.037

AD+

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size
A4

Document Number

Husk/Petra

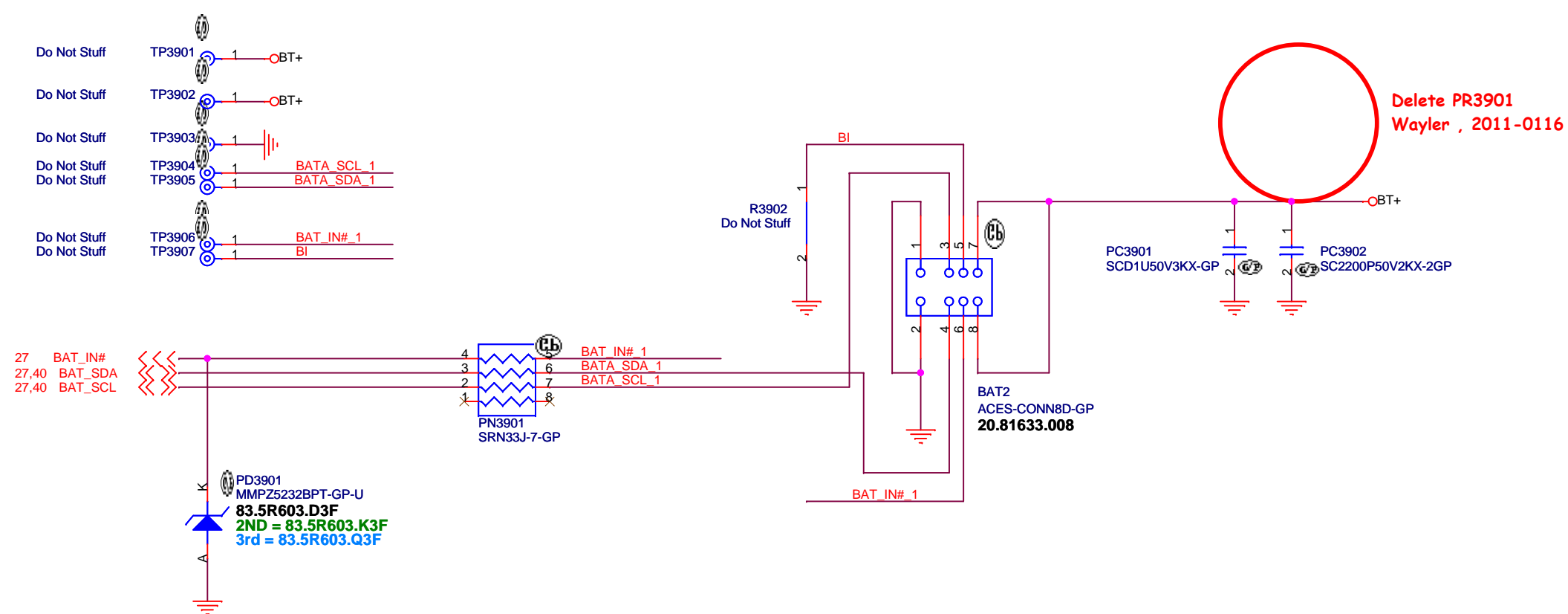
Rev

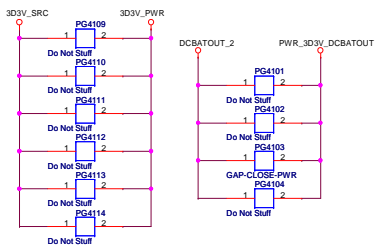
-4M

Date: Thursday, September 06, 2012

Sheet 38 of 103

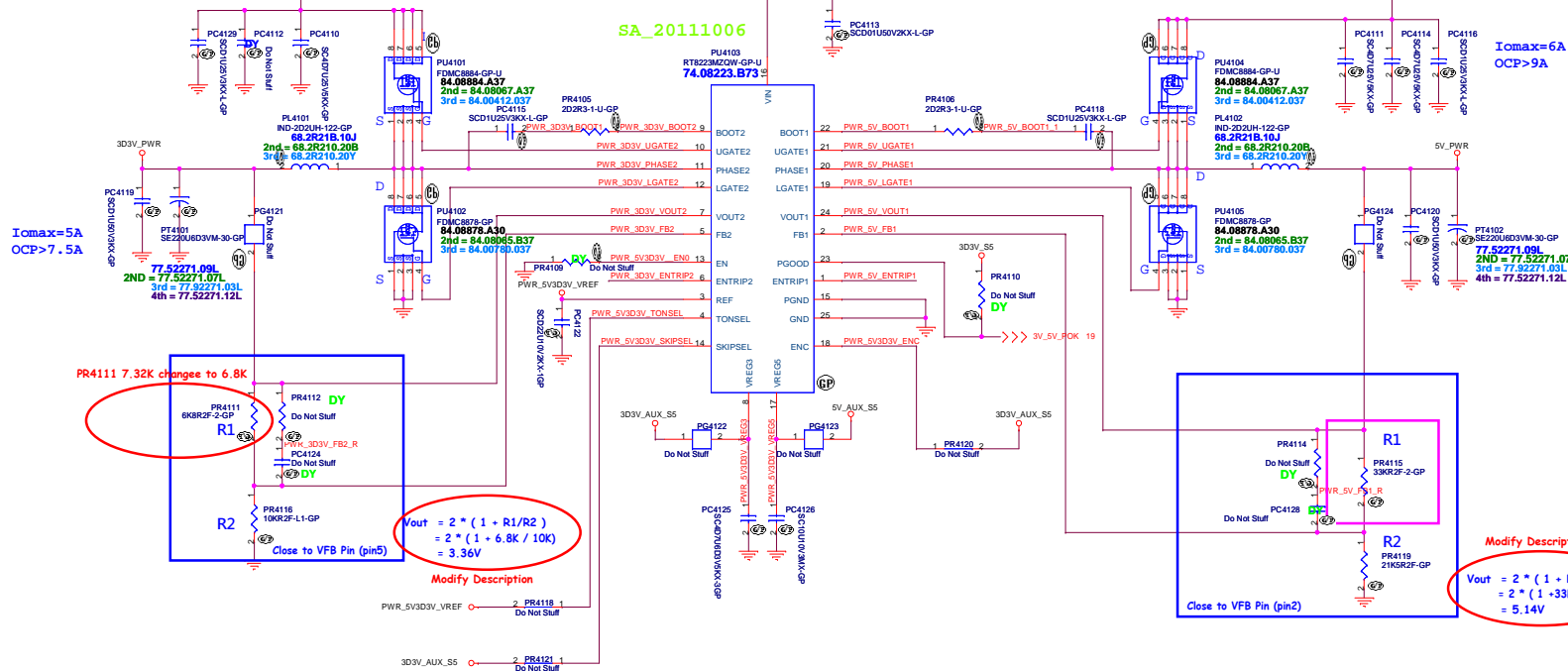
BATTERY CONNECTOR





SA_20111004

PWR_3D3V_DCBATOUT



I_{omax}=5A
OCP>7.5A

I_{omax}=6A
OCP>9A

Modify Description

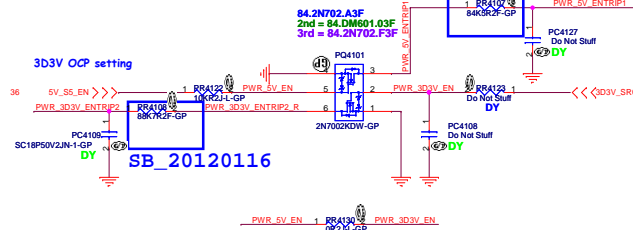
$$V_{out} = 2 * (1 + R1/R2) = 2 * (1 + 33K / 21K) = 5.14V$$

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

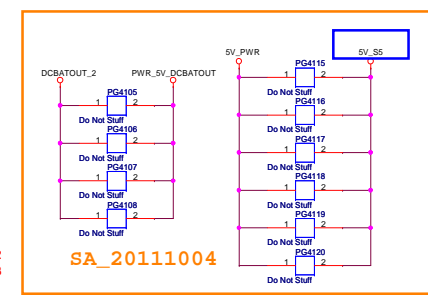
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

SB_20120116

5V OCP setting



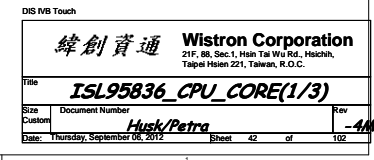
SB_20120116

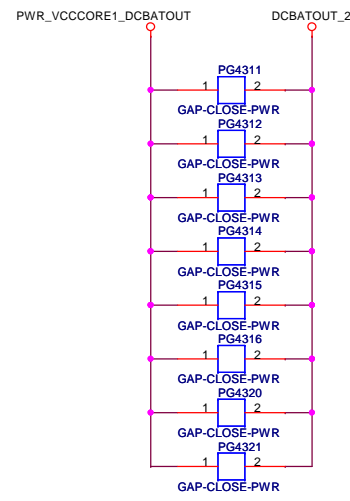
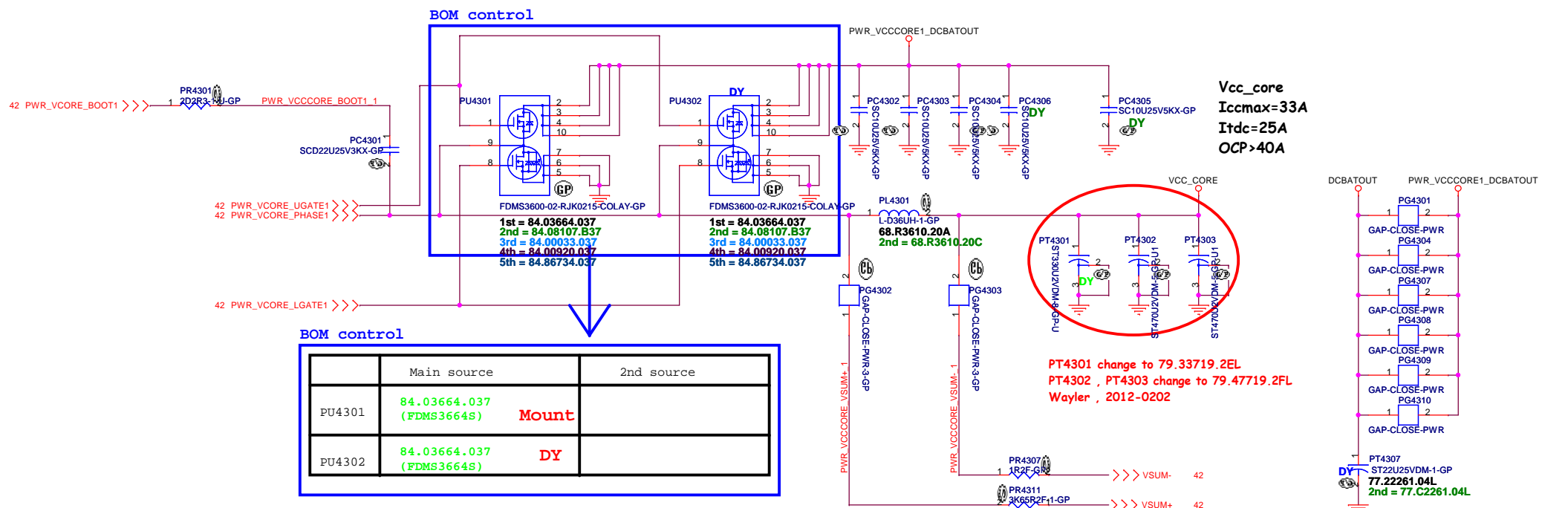


SA_20111004

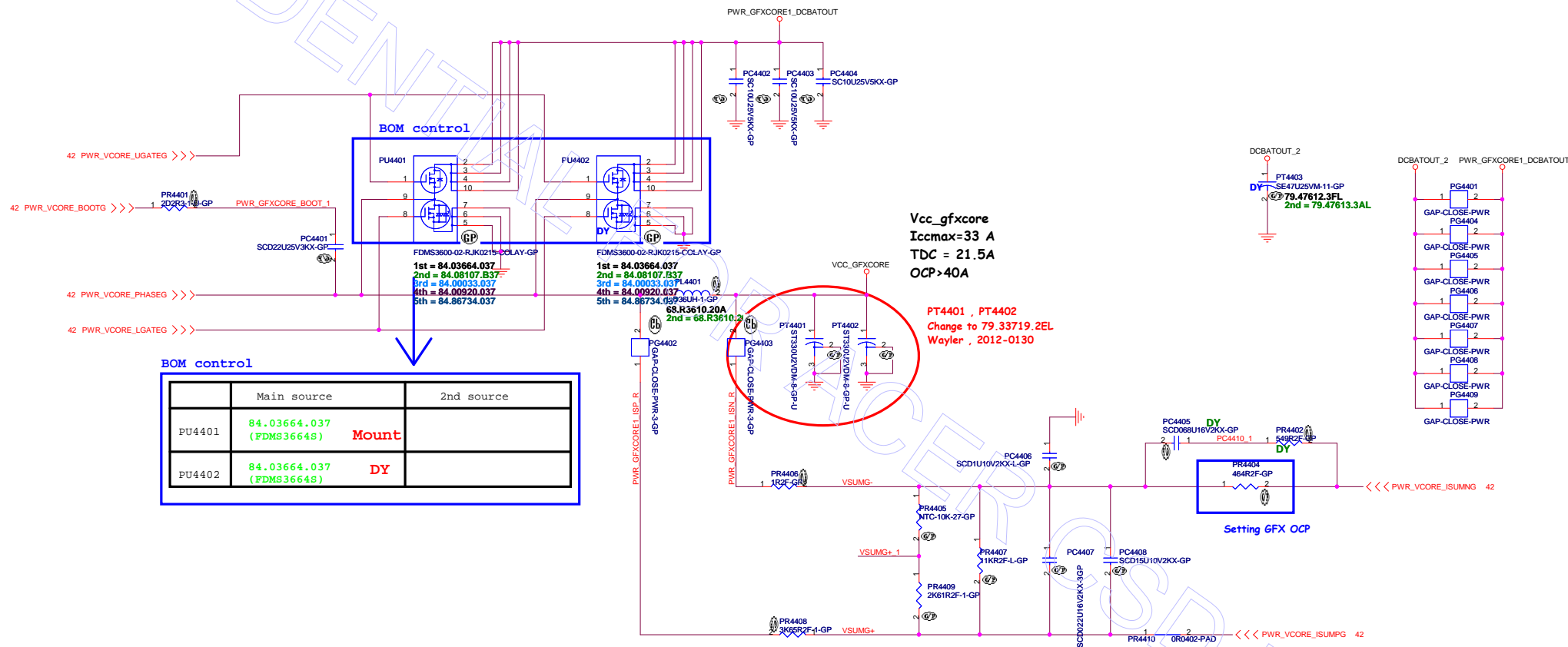
DIS IWB Touch

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CONFIDENTIAL



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

Vcc_gfxcore
Iccmax=33 A
TDC = 21.5A
OCP>40A

PT4401 , PT4402
Change to 79.33719.2EL
Wayler , 2012-0130

Setting GFX OCP

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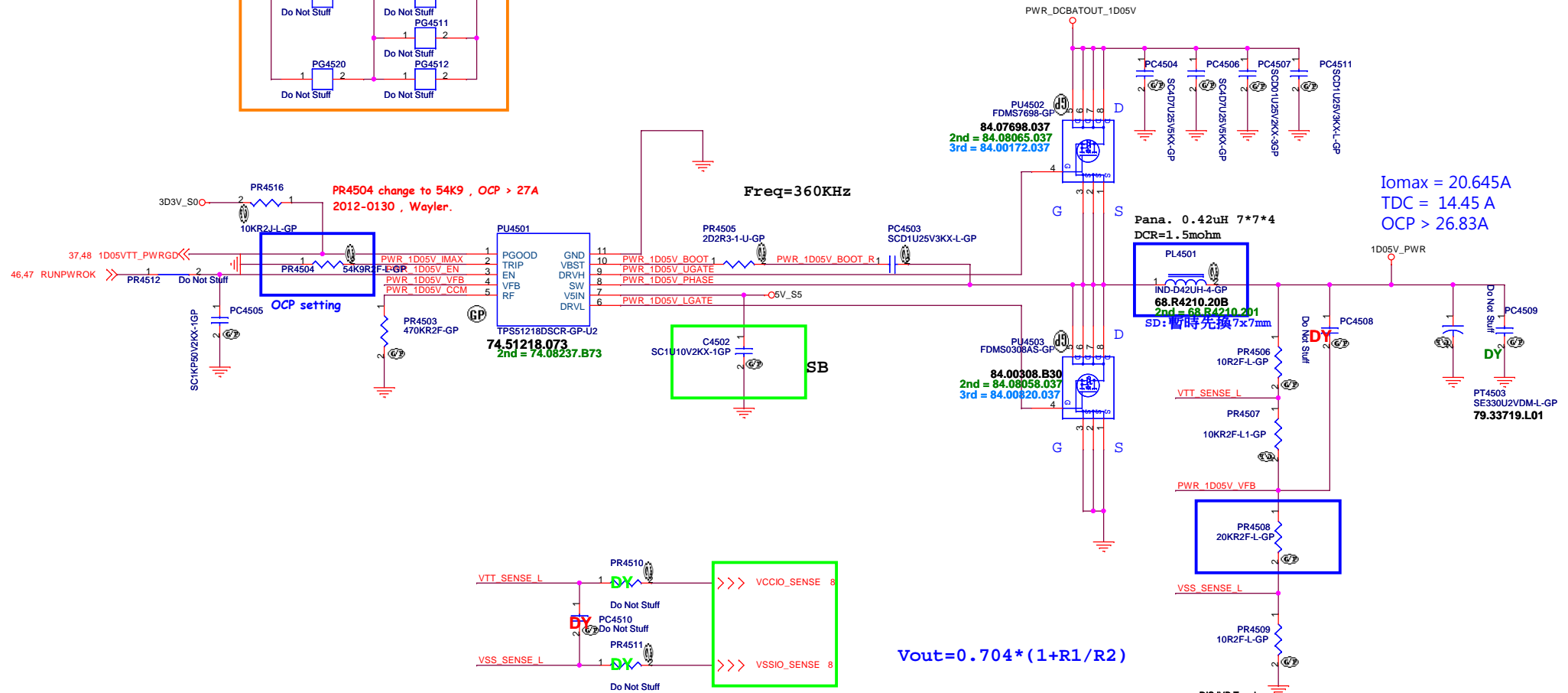
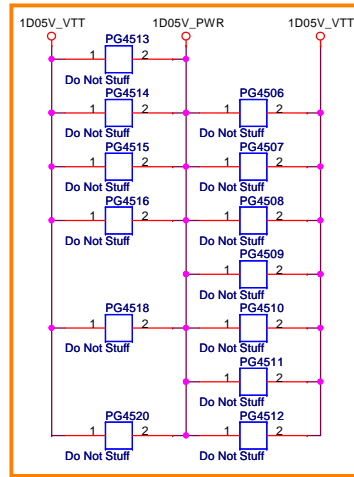
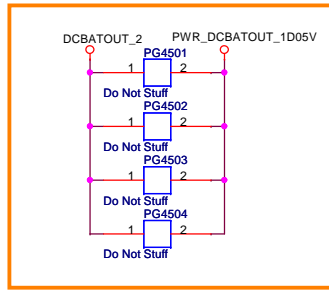
緯創資通 Wistron Corporation
21F, 83, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ISL95836_CPU_CORE(3/3)
Size	Document Number	Rev	
Custom		Husk/Petra	
Date:	Monday, September 17, 2012	Sheet	44 of 102

SA_20111004

SA_20111013

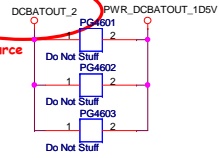
TPS51218D for 1D05V



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
DC to DC 1D05V(TPS51218D)		
Size	Document Number	Rev
A3	Husk/Petra	-4M
Date: Thursday, September 06, 2012		
Sheet 45 of 103		

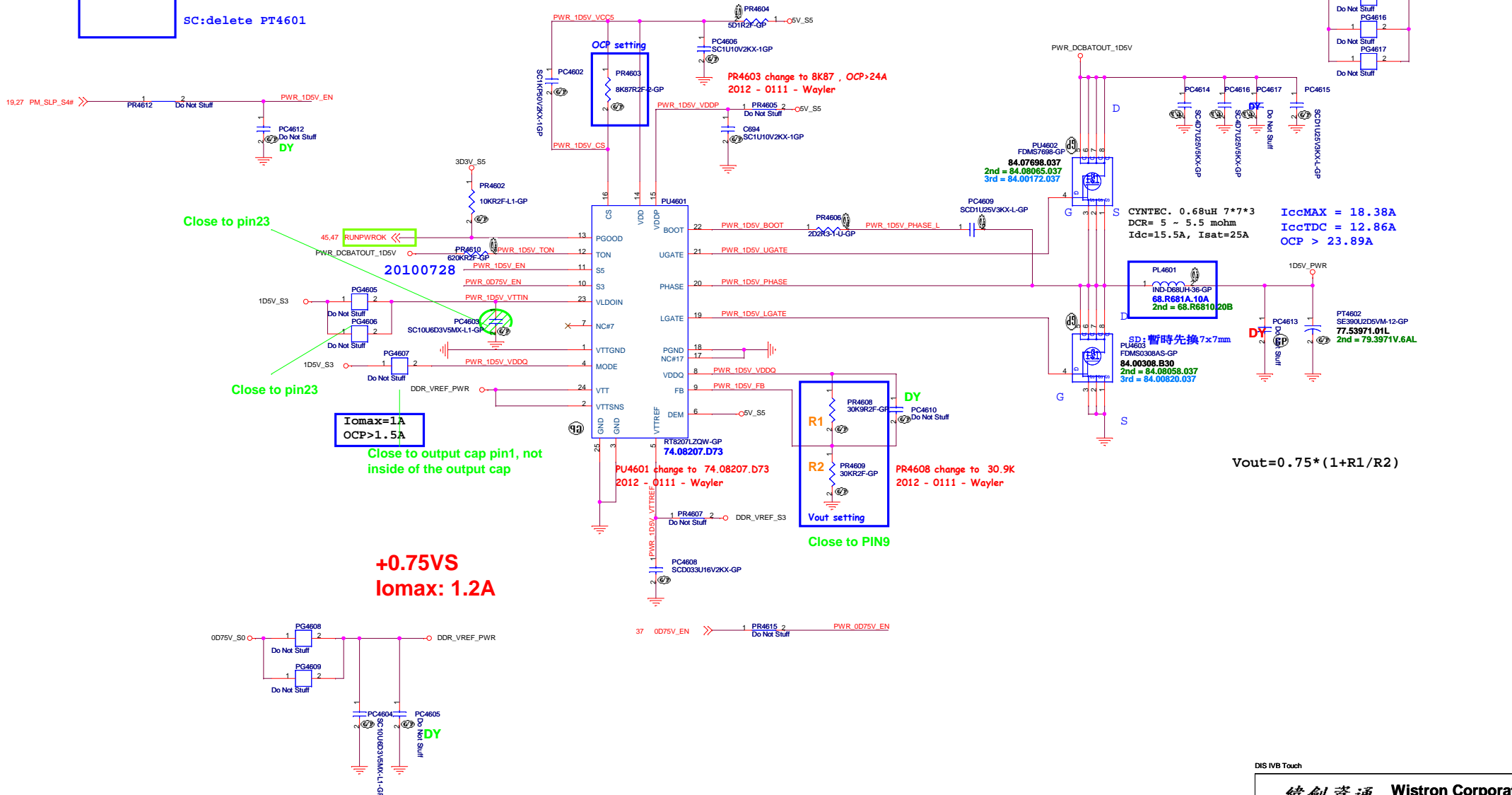
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SSID = PWR.Plane.Regulator_1p5v0p75v
```



SA_20111004

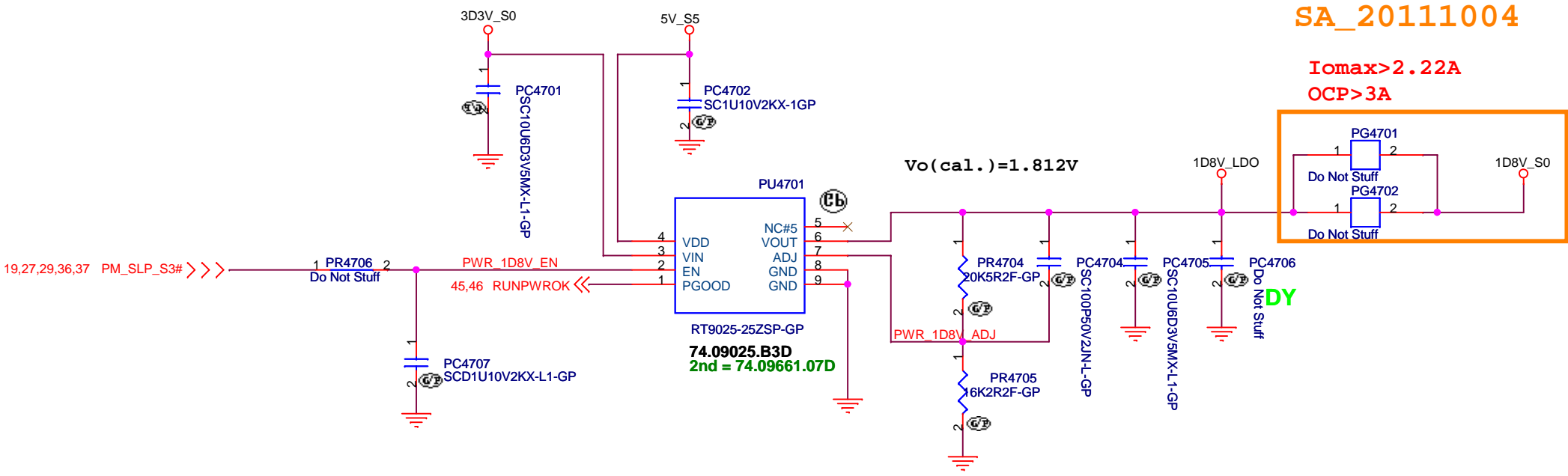
```
SC:delete PT4601
```

RT8207L for 1D5V


$$V_{out} = 0.75 * (1 + R1/R2)$$

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



SA_20111004

Iomax>2.22A
OCP>3A

DIS IVB Touch

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LDO 1D8V(RT9025)			
Size	Document Number		Rev
A4	Husk/Petra		-4M
Date:	Thursday, September 06, 2012		Sheet 47 of 103

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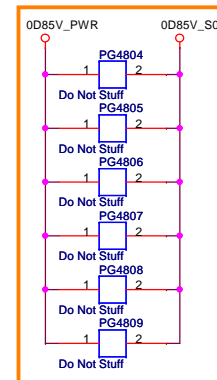


D0	D1	V _O , MODE=0	V _O , MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

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```
pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"
```



97 DBC_I

97 BLON_

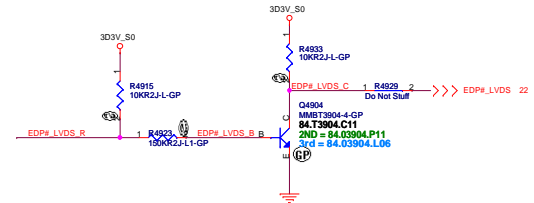
97 LCD_BRIGHTNESS

57 DF_TXFT_CF

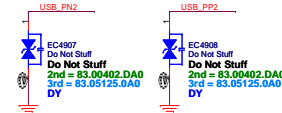
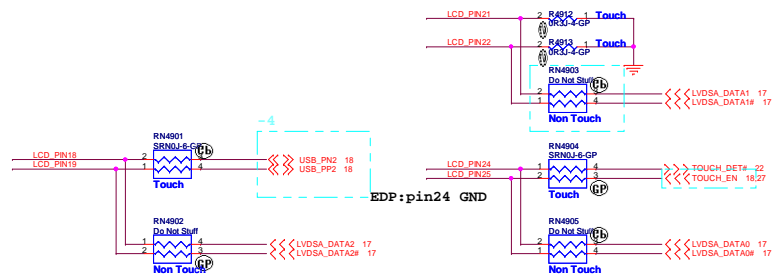
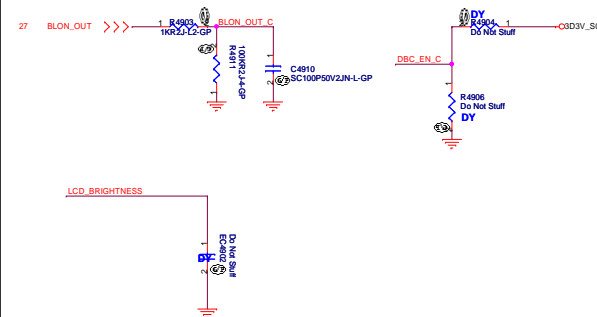
07.09.2020.00

97 DP_TXN0_CP

97 DP_DDC_CLK

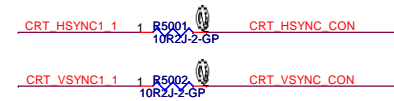
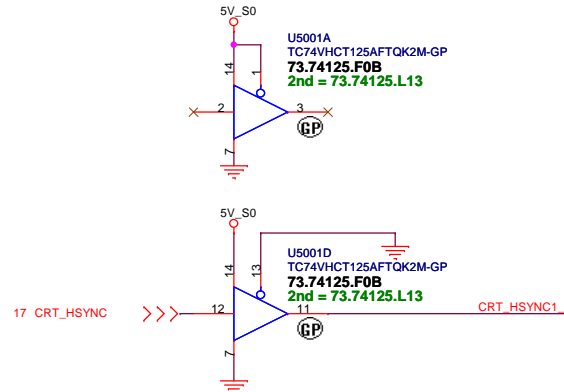
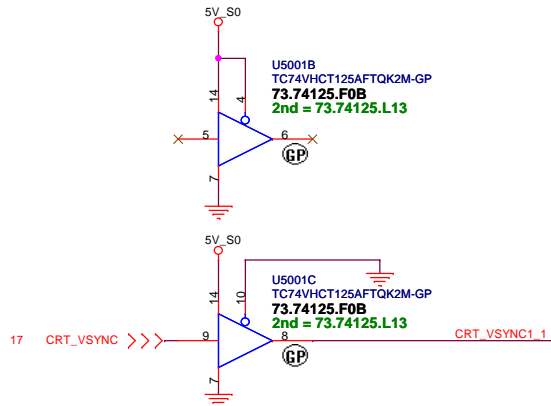
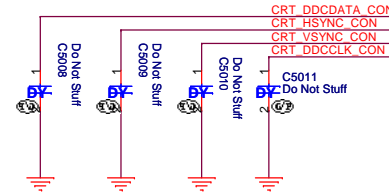
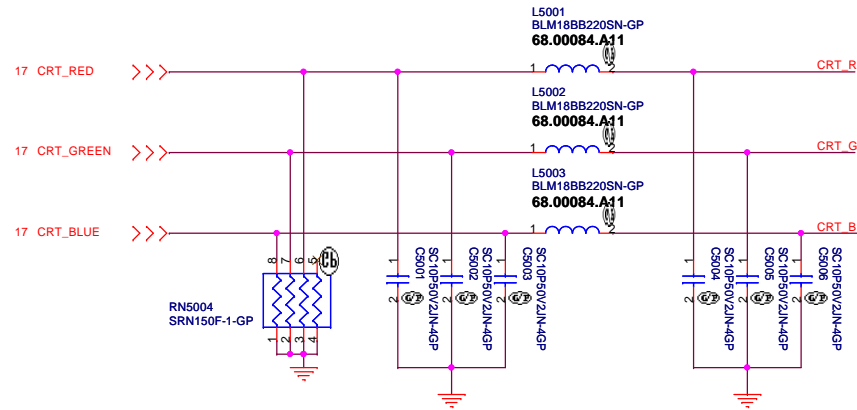
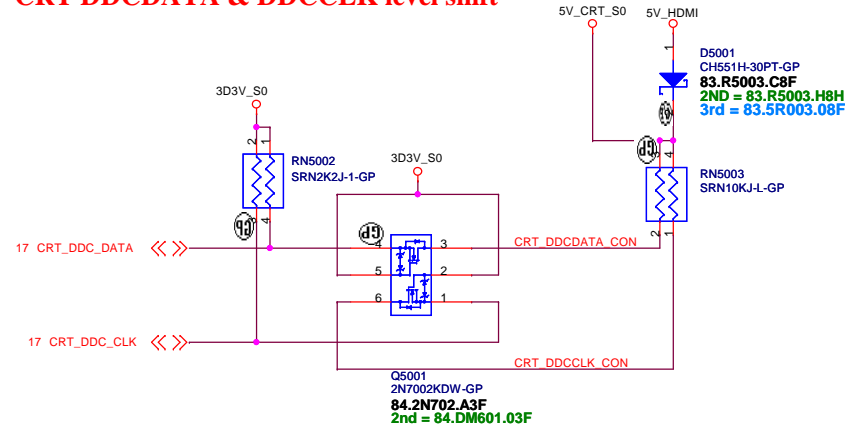


Layout 40 mil



CRT DDCDATA & DDCCLK level shift

CRT_DDCDATA_CON >>> CRT_DDCDATA_CON 59
 CRT_DDCCLK_CON >>> CRT_DDCCLK_CON 59
 CRT_R >>> CRT_R 59
 CRT_G >>> CRT_G 59
 CRT_B >>> CRT_B 59
 CRT_HSYNC_CON >>> CRT_HSYNC_CON 59
 CRT_VSYNC_CON >>> CRT_VSYNC_CON 59



DIS IVB Touch

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size	Document Number	Rev
A3	Husk/Petra	-4M
Date:	Thursday, September 06, 2012	Sheet 50 of 103

HDMI Level Shifter & CONNECTOR

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm



DIS IVB Touch

Title	
eDP	
Size	Document Number
A3	Husk/Petra
Date:	Thursday, September 06, 2012
Sheet	52 of 103
Rev	
-4M	

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

(Blanking)

DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>S-VIDEO</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 53 of 103

(Blanking)

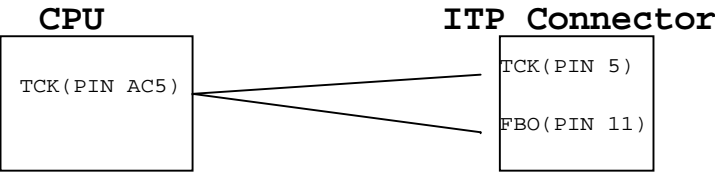
DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

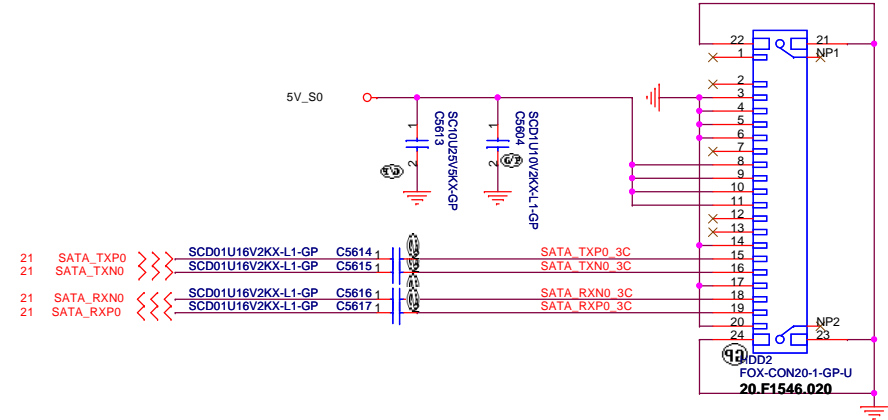
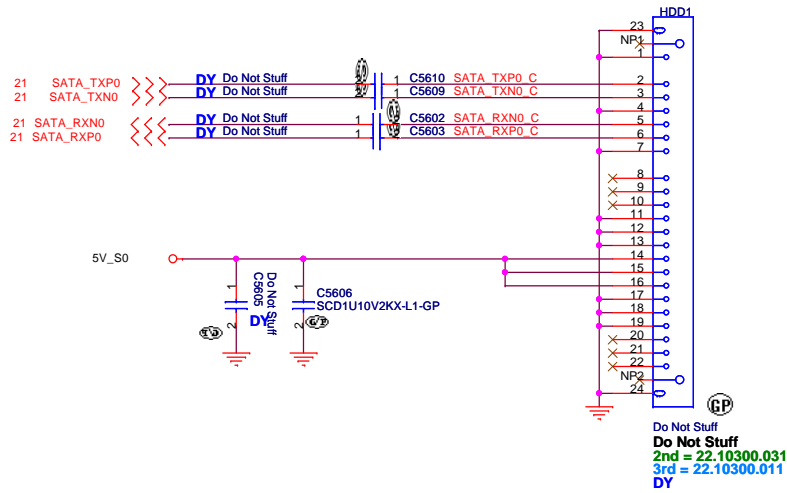


DIS IVB Touch

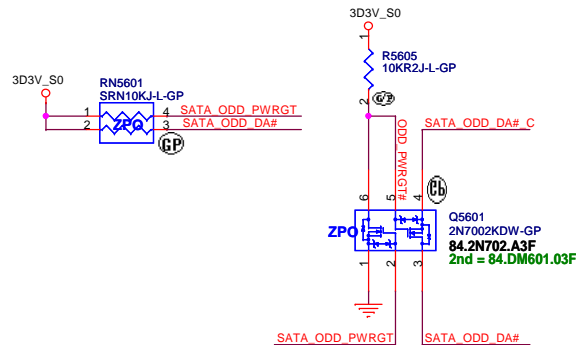
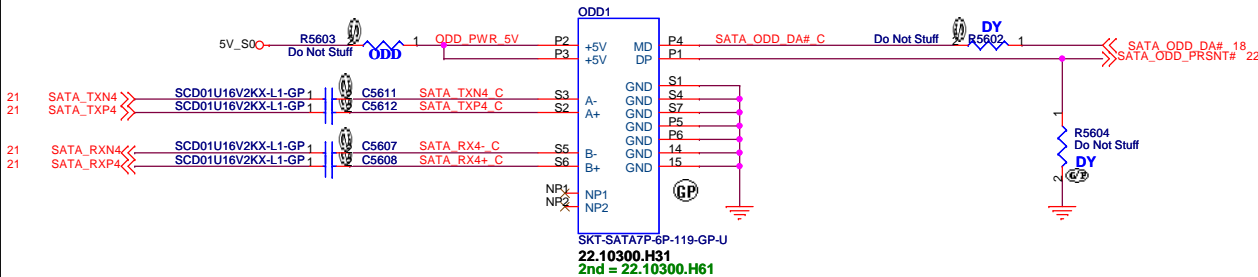
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP			
Size	Document Number		Rev
A4	Husk/Petra		-4M
Date: Thursday, September 06, 2012		Sheet 55 of	103

SSID = SATA

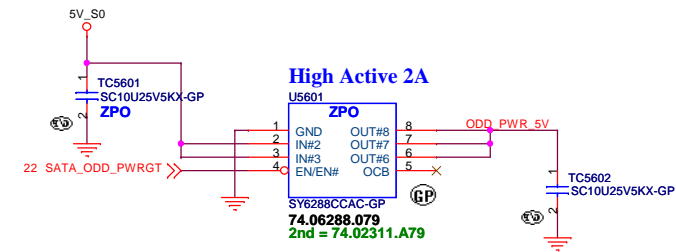
SATA HDD Connector



ODD Connector



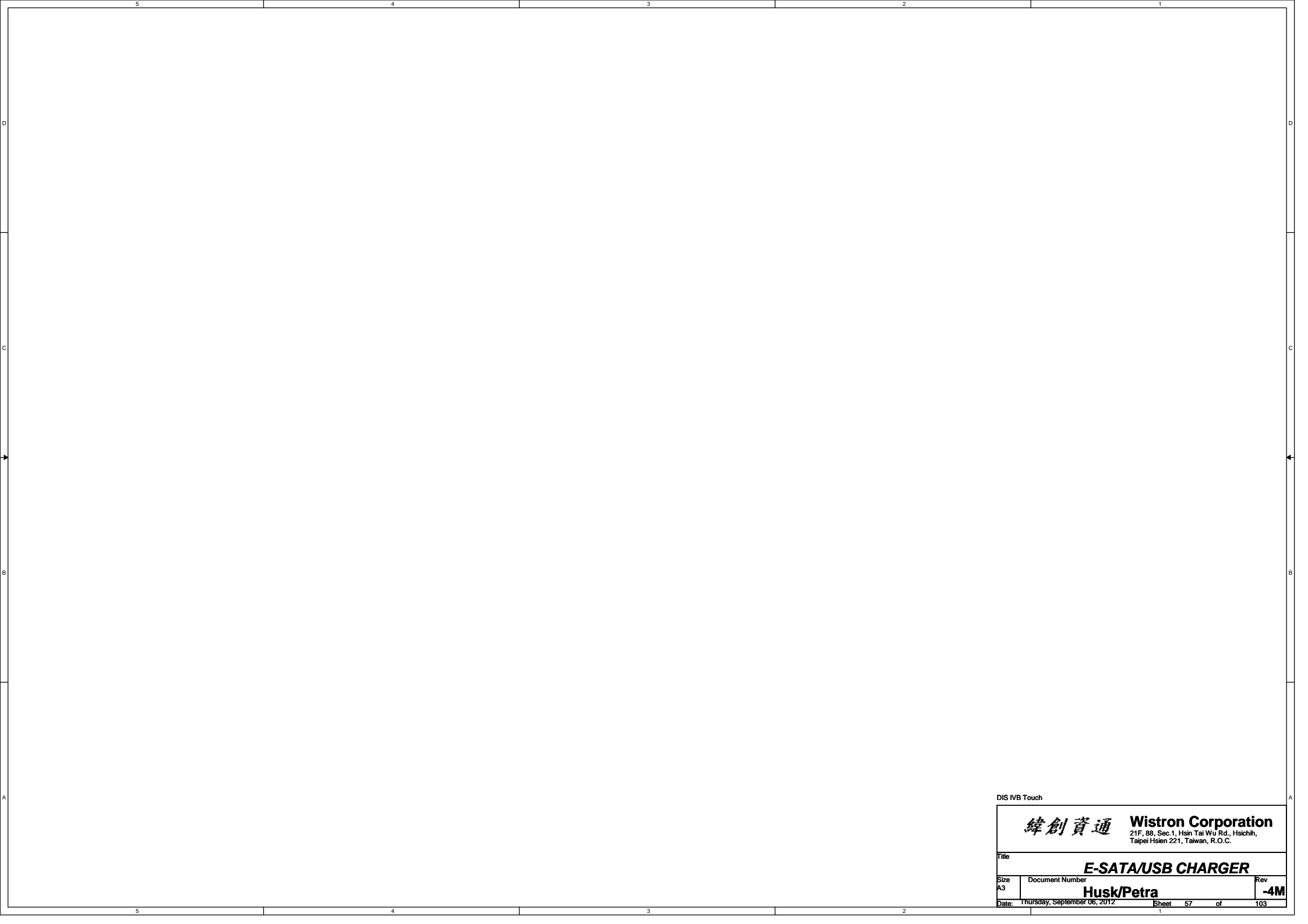
SATA Zero Power ODD



DIS I/B Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD/ODD			
Size	Document Number	Rev	
A3			-4M
Date:	Thursday, September 06, 2012	Sheet	56 of 103



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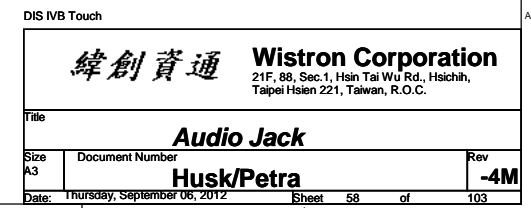
B

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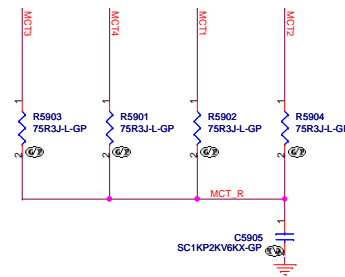
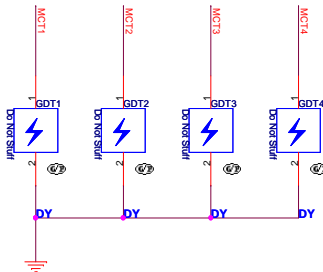
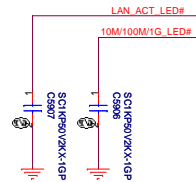
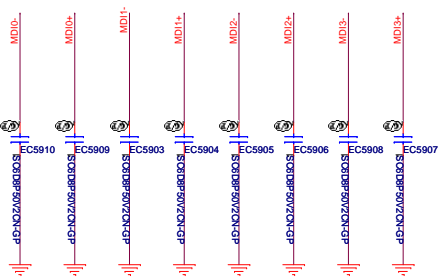
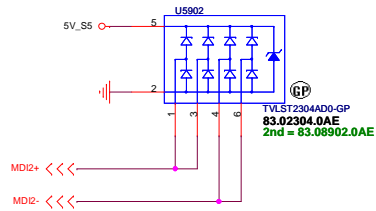
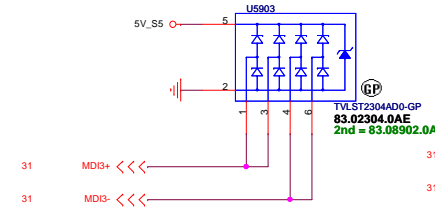
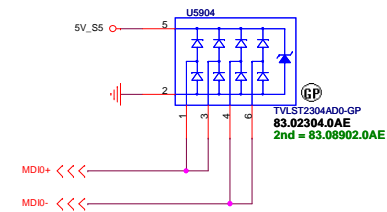
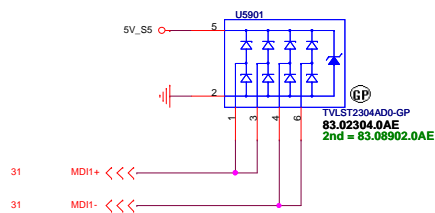
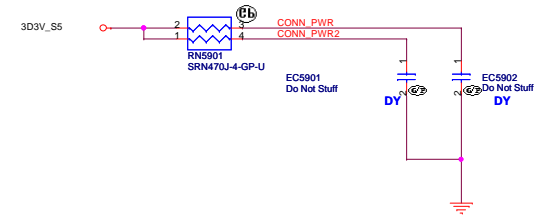
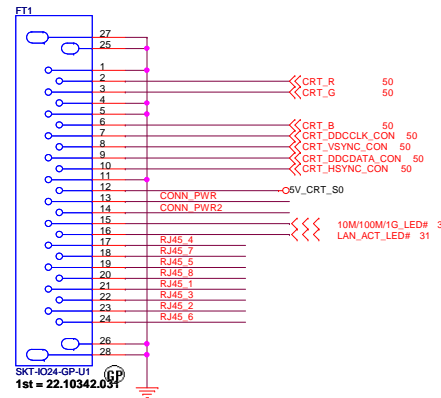
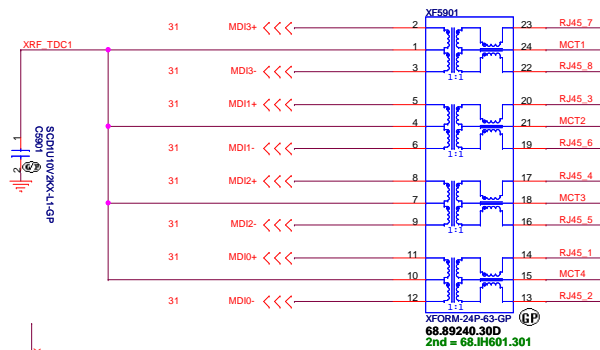
DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
A3	Husk/Petra	-4M
Date:	Thursday, September 06, 2012	Sheet 57 of 103

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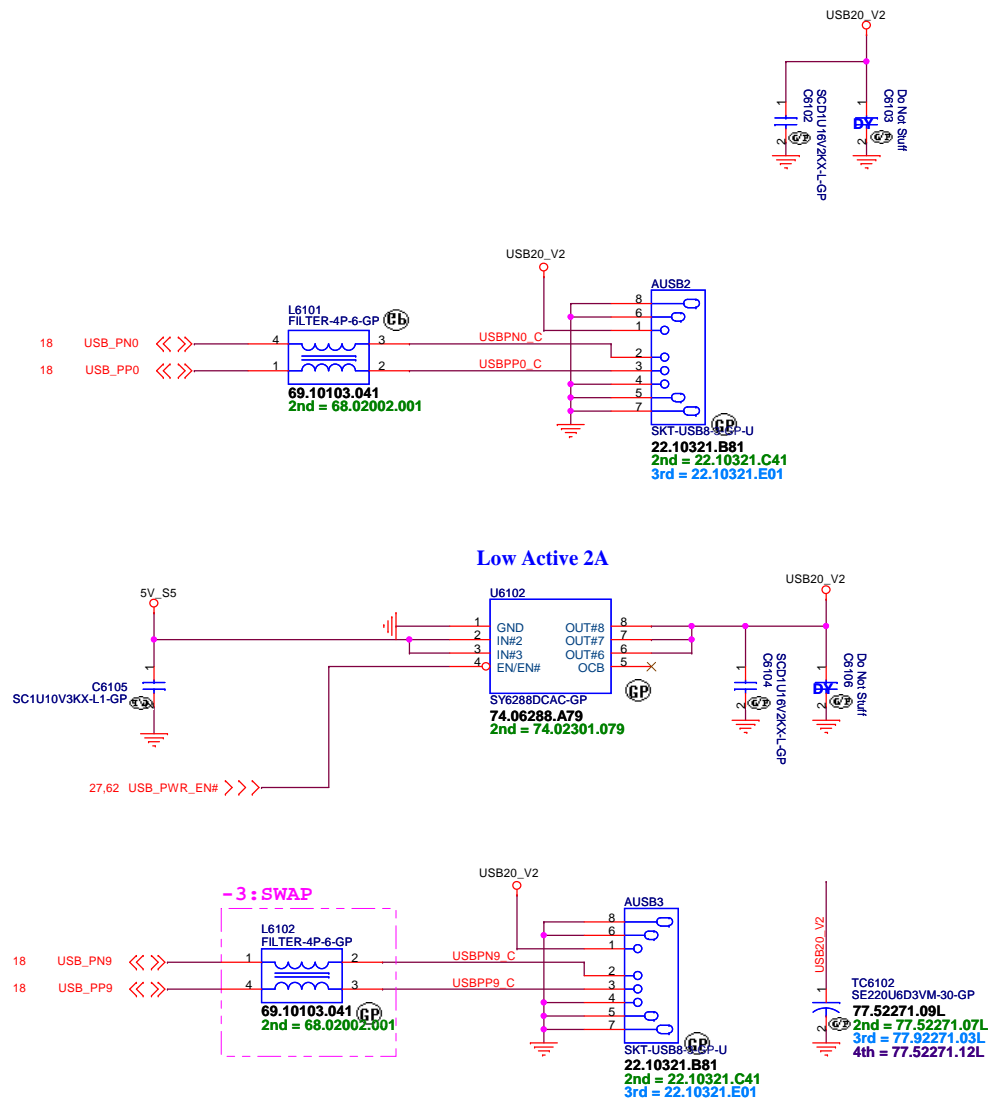


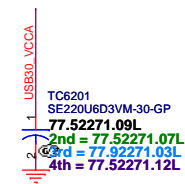
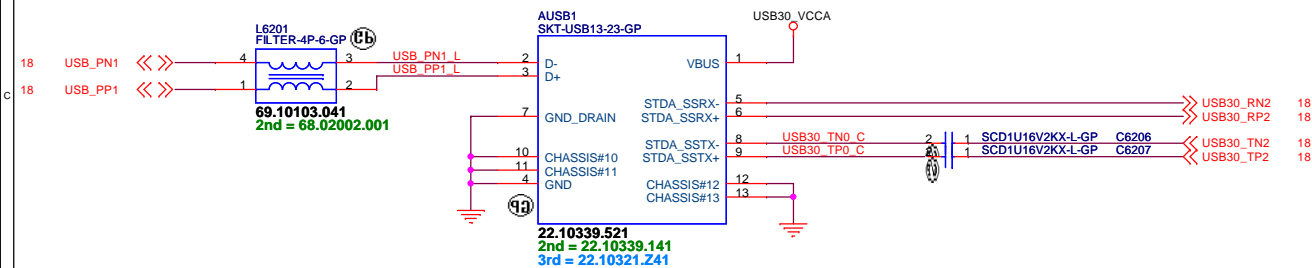
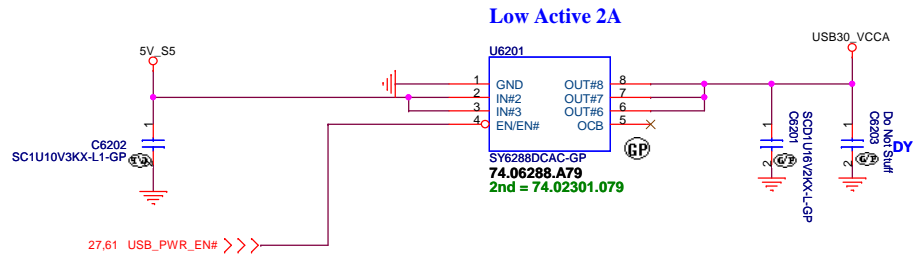
SSID = LAN



DIS I/B Touch

SSID = USB





USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title			USB 3.0 Port		
Size	Document Number				Rev
A3	Husk/Petra				-4M
Date:	Thursday, September 13, 2012				Sheet 62 of 103

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

DIS IVB Touch

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Bluetooth

Size
A4

Document Number

Husk/Petra

Rev
-4M

Date: Thursday, September 06, 2012

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DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>RESERVED</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 64 of 103

Mini Card Connector(802.11a/b/g/n)



Title			
MINICARD(WLAN)/ITP CONN			
Size A3	Document Number		Rev
	Husk/Petra		-4M
Date:	Friday, December 21, 2012	Sheet 65 of	103

SSID = Wireless

Mini Card Connector(WWAN)

DIS IVB Touch

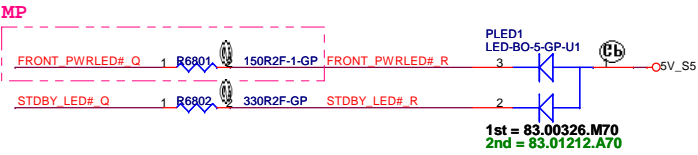
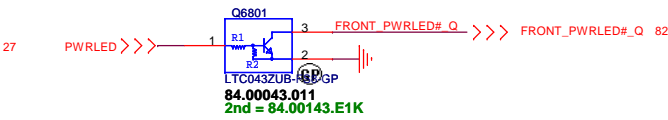
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>WWAN Connector</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 66 of 103

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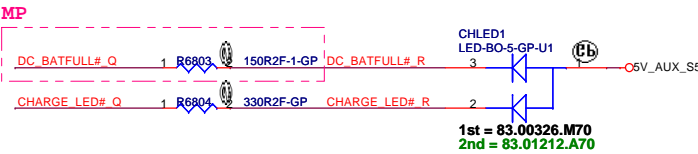
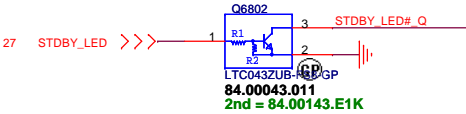
DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 67 of 103

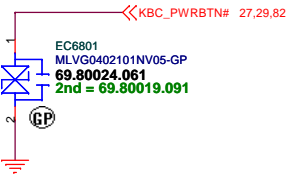
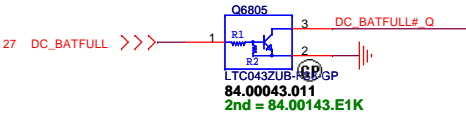
Power button LED



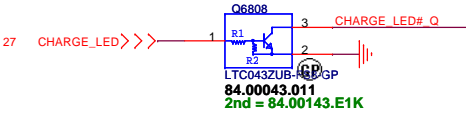
Power STDBY_LED



Battery LED2(DC_BATFULL)



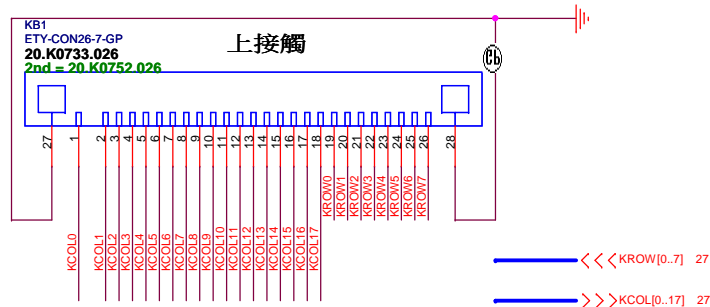
Battery LED1(CHARGE)



DIS IVB Touch			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED Bard/Power Button			
Size	Document Number		Rev
Custom	Husk/Petra		-4M
Date:	Thursday, September 06, 2012	Sheet 68 of	103

SSID = KBC

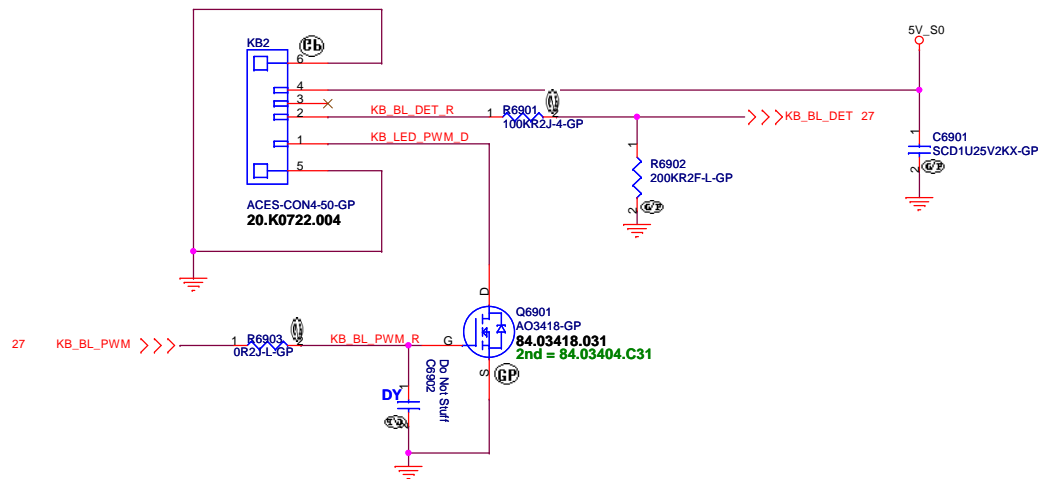
Internal KeyBoard Connector



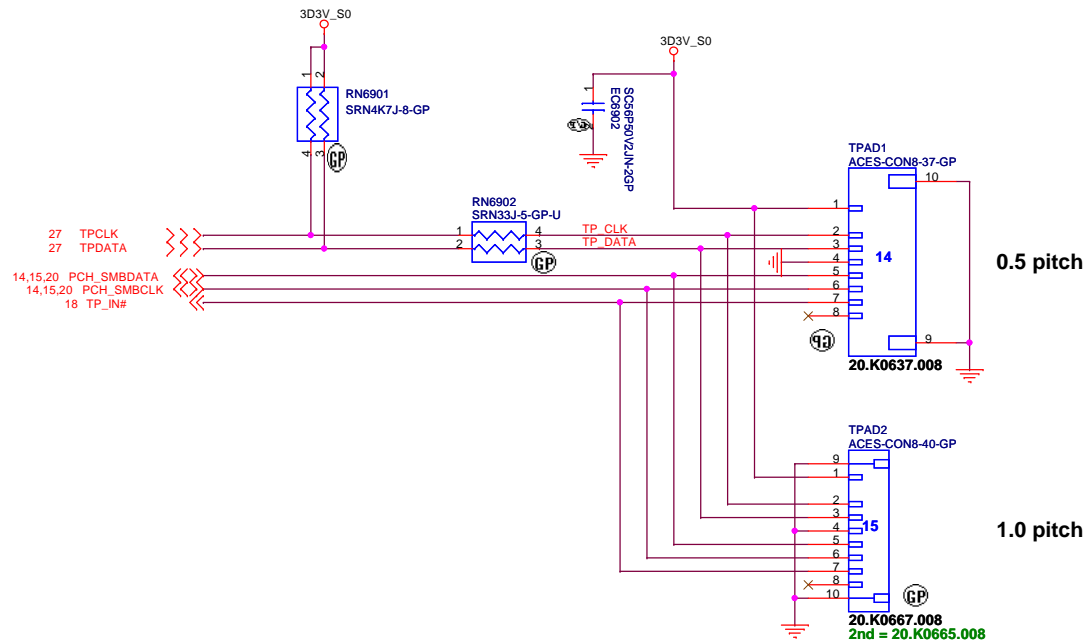
R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

VIEW FROM TOP SIDE

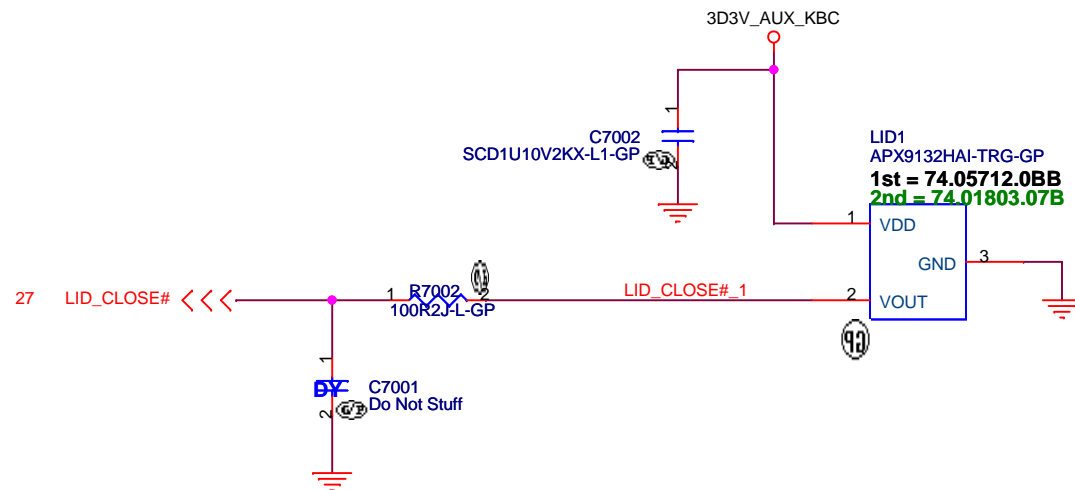
PIN NUMBER



TOUCH PAD



DIS IVB Touch



DIS IVB Touch

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

Document Number

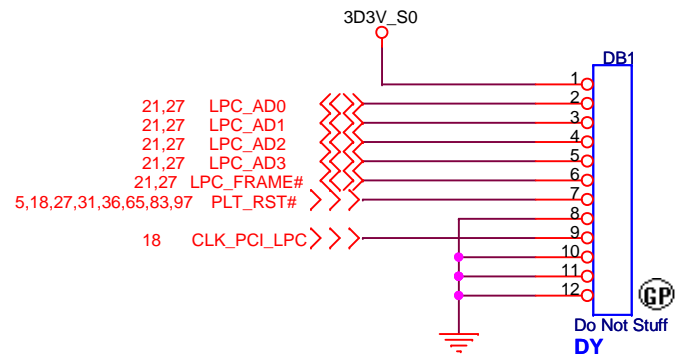
Husk/Petra

Rev

-4M

Date: Thursday, September 06, 2012

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DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Dubug connector</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 71 of 103

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<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleReserved		
SizeA3	Document NumberHusk/Petra	Rev-4M
Date: Thursday, September 06, 2012	Sheet72	of103

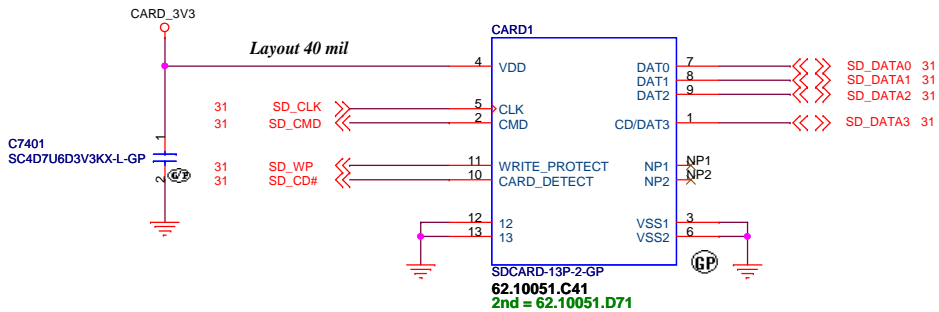
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DIS IVB Touch

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>Husk/Petra</div>		<div>-4M</div>
<div>Date:</div>	<div>Thursday, September 06, 2012</div>		<div>Sheet 73 of 103</div>

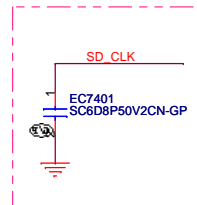
SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_RE#	xD_CE#
SP3	SP3	SD_D5	MS_WE#	xD_D6
SP4	SP4	SD_D4	MS_CLK	xD_D5
SP5	SP5	SD_D3	MS_D7	xD_D4
SP6	SP6	SD_D2	MS_D6	xD_D3
SP7	SP7	SD_D1	MS_D5	xD_D2
SP8	SP8	SD_D0	MS_D4	xD_D1
SP9	SP9	SD_WP	MS_CD#	xD_CD#
SP10	SP10	SD_CD#	MS_D5	xD_D0
SP11	SP11	SD_WP	MS_D4	xD_D1
SP12	SP12	SD_CD#	MS_D0	xD_CD#
SP13	SP13	SD_WP	MS_D1	xD_WP#
SP14	SP14	SD_CD#	MS_D5	xD_ALE
SP15	SP15	SD_WP	MS_D4	xD_D0
SP16	SP16	SD_CD#	MS_D0	xD_D1

-2:EMI



DIS IVB Touch

緯創資通

Wistron Corporation

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Title

CARD Reader CONN

Size
Custom

Document Number

Husk/Petra

Rev

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

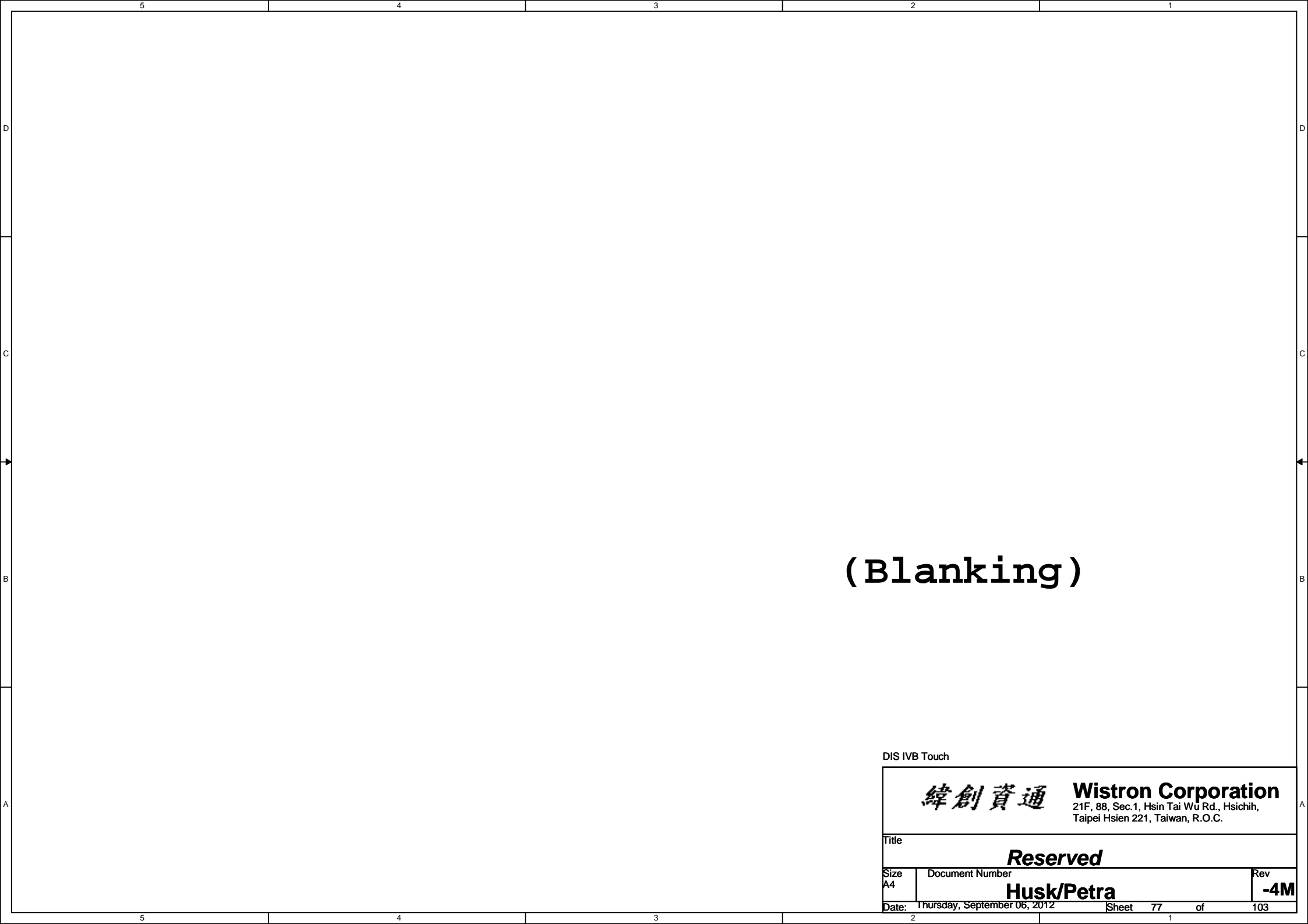
DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
New Card		
Size	Document Number	Rev
A3	Husk/Petra	-4M
Date:	Thursday, September 06, 2012	
	Sheet	75 of 103

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DIS IVB Touch

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 76 of 103



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DIS IVB Touch

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<div>Reserved</div>			
Size A4	Document Number <div>Husk/Petra</div>		Rev <div>-4M</div>
Date:	Thursday, September 06, 2012	Sheet 77 of	103

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DIS IVB Touch

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleReserved		
SizeA4	Document NumberHusk/Petra	Rev-4M
Date: Thursday, September 06, 2012		Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

DIS IVB Touch

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

G- Sensor

Size
A4

Document Number

Husk/Petra

Rev

-4M

Date: Thursday, September 06, 2012

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5

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DIS IVB Touch

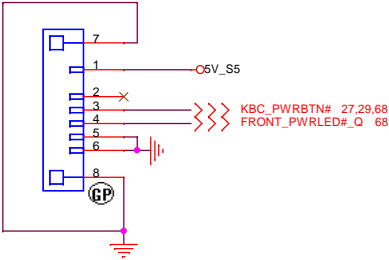
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
Date: Thursday, September 06, 2012		Sheet 80 of 103

(Blanking)

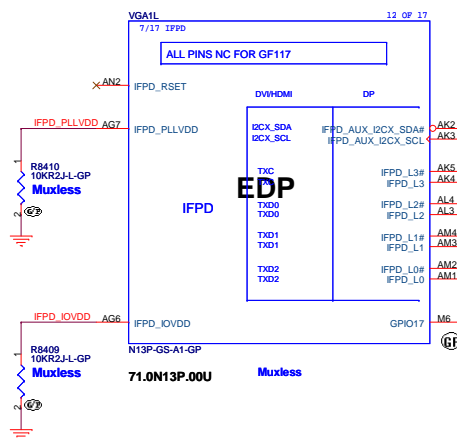
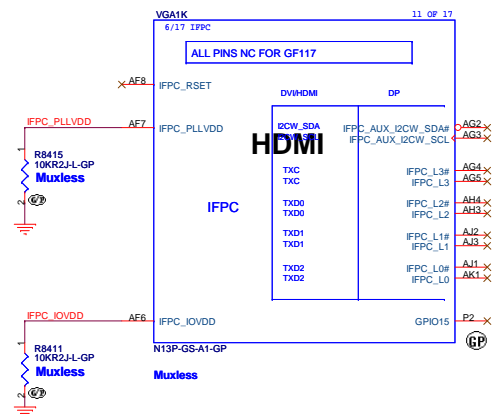
DIS IVB Touch

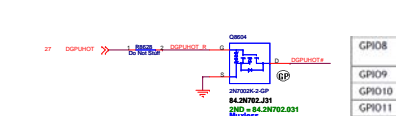
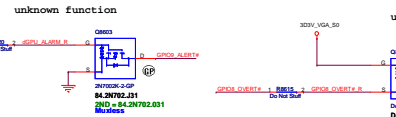
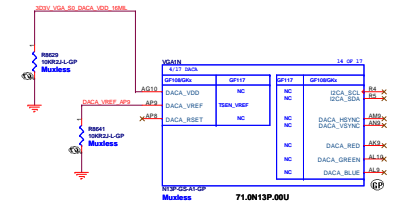
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
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PWRCN1
ACES-CON6-52-GP
20.K0721.006
2nd = 20.K0382.006



DIS IVB Touch		
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TitleIO Board Connector		
SizeA3	Document NumberHusk/Petra	Rev-4M
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GPIO	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO8	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	I/O	Memory VREF Control
GPIO11	GPU_VDD	O	GPU Core VDD VDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw Input

VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0011(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm
64.49915.6DL

10Kohm
64.10025.1.0L

VRAM Table(N13M-GS/NS)

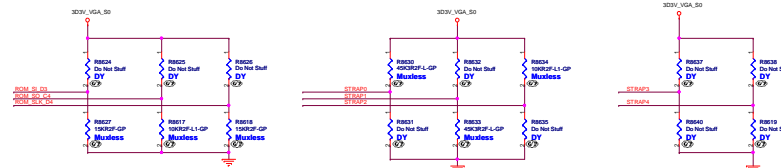
Hynix 2G_D-die 1100(0xC) 128*16	Hynix 1G_B-die 0110(0x6) 128*16
---------------------------------------	---------------------------------------

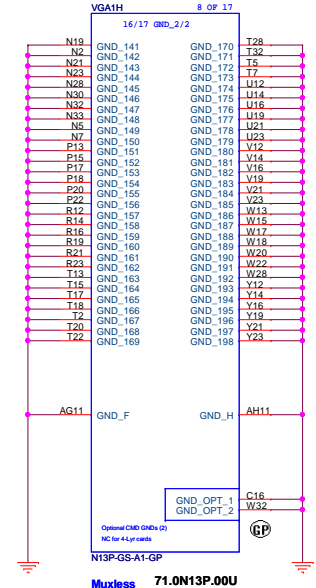
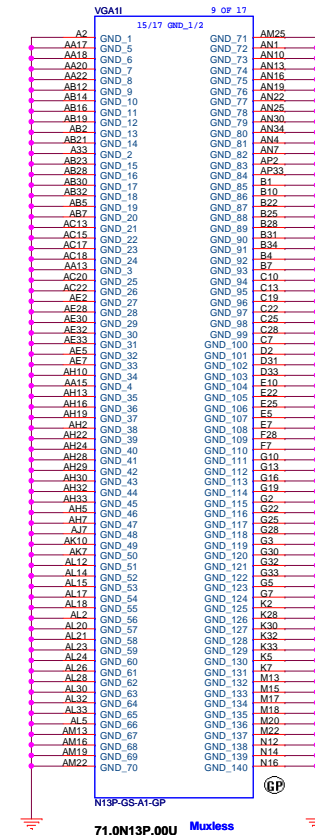
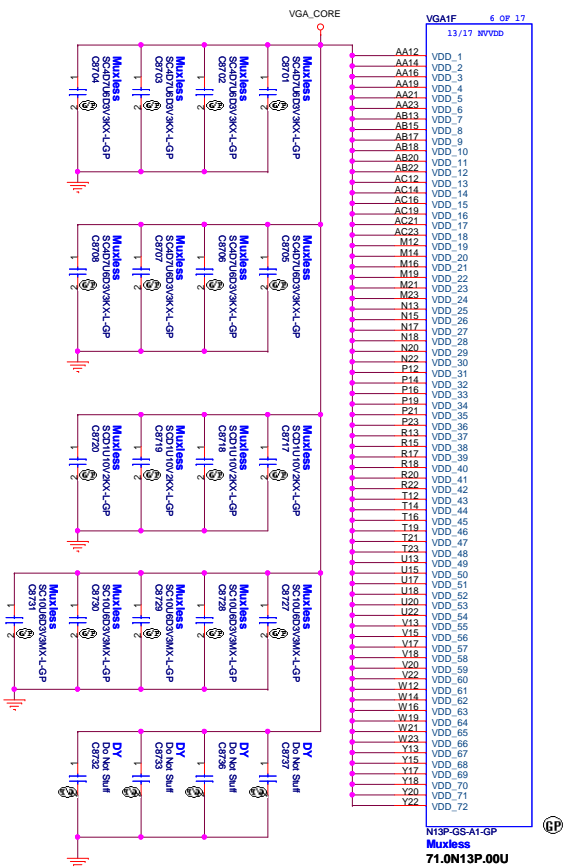
Logical Strap Bit Mapping	Resistor	Pull-up	Pull-down
50kOhm	1001	0001	
100kOhm	1001	0001	
150kOhm	1010	0010	
200kOhm	1011	0011	
250kOhm	1100	0100	
300kOhm	1101	0101	
350kOhm	1110	0110	
400kOhm	1111	0111	

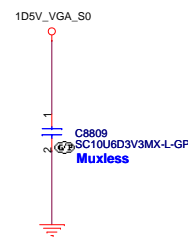
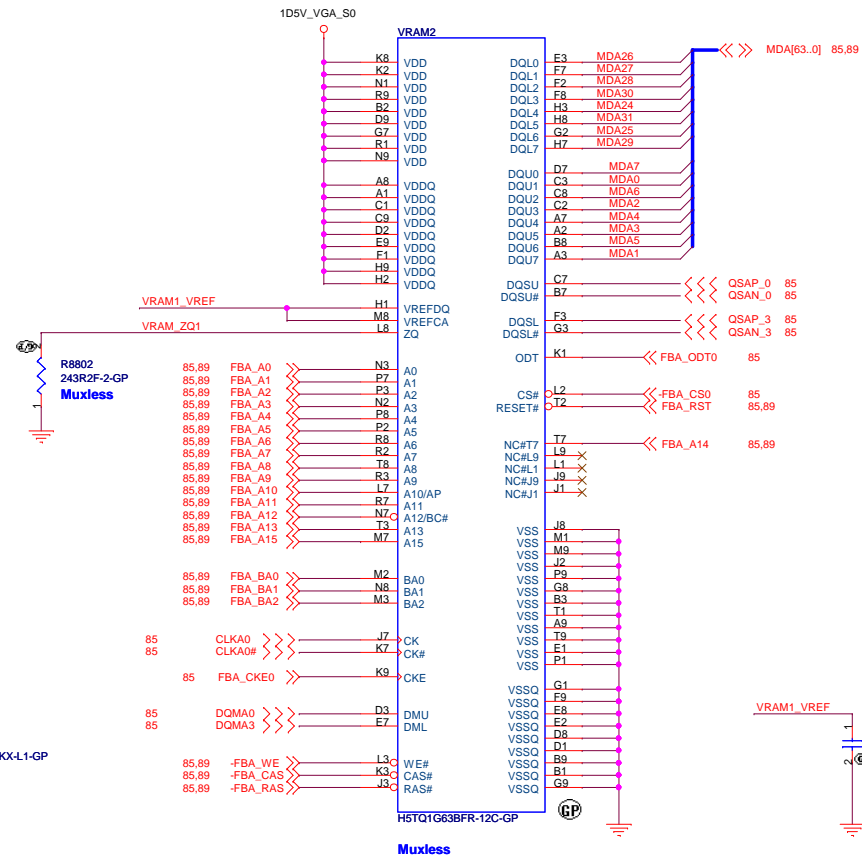
Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVDD (V)
MAX Point (MP)	H13P-GL/-HS1	800	900	--
	H13P-GLP	660	900	--
TDP Point (TP)	H13P-GL/-HS1	660	900	--
	H13P-GLP	475	900	--
HW Boot Voltage	H13P-GL/-HS1	--	--	0.95
	H13P-GLP	--	--	0.90

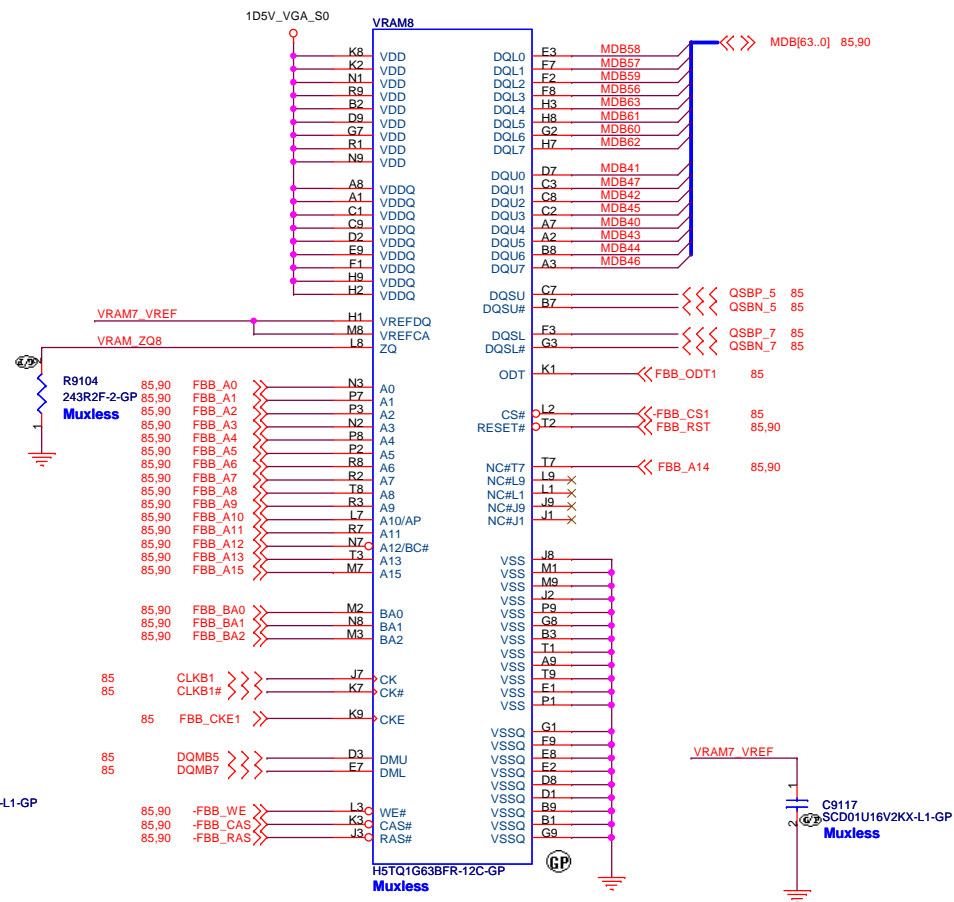
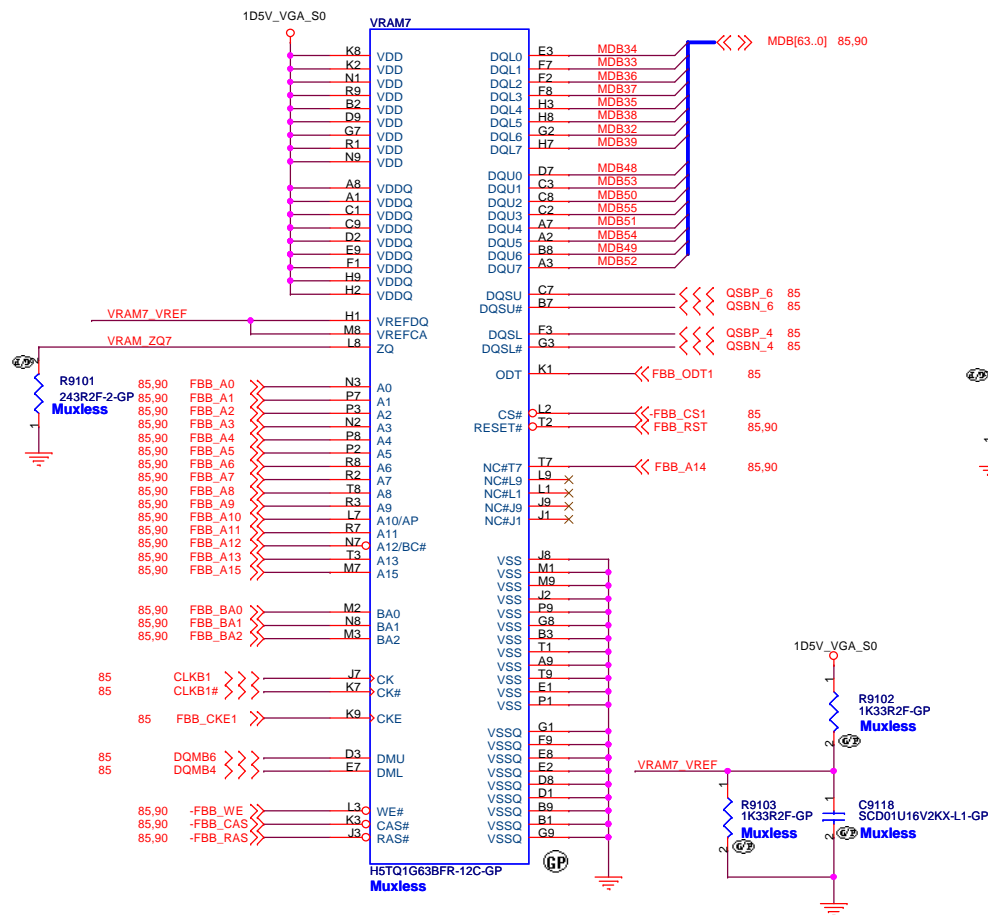
Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0
ROM.SOLK	PCI.DEVID[4]	SUB.VENDOR	SLOT.CLK.CFG/	PEX.PLL.ENTERM
	0	0	1	0
ROM.SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]
	0	0	0	0
ROM.SO	XCLK.417	FB.0.BAR.SIZE	SMB.ALT.ADDR	VGA.DEVICE
	0	0	0	1
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
	1	1	1	1
STRAP1	3GIO.PADCFG[5]	3GIO.PADCFG[2]	3GIO.PADCFG[1]	3GIO.PADCFG[0]
	0	1	1	1
STRAP2	PCI.DEVID[3]	PCI.DEVID[2]	PCI.DEVID[1]	PCI.DEVID[0]
	1	0	0	1
STRAP3	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	N/A

15K ohm pull-down
10K ohm pull-down
45K ohm pull-up
45K ohm pull-down
10K ohm pull-up

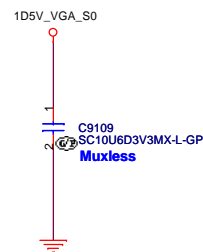








FOR VRAM7

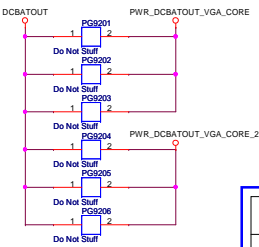


FOR VRAM8

DIS IVB Touch

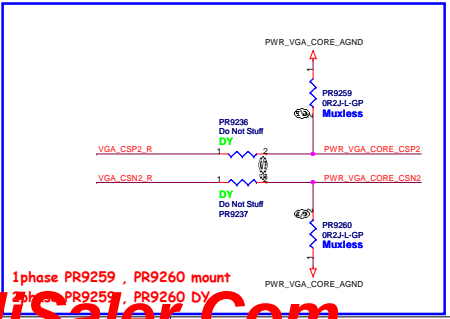
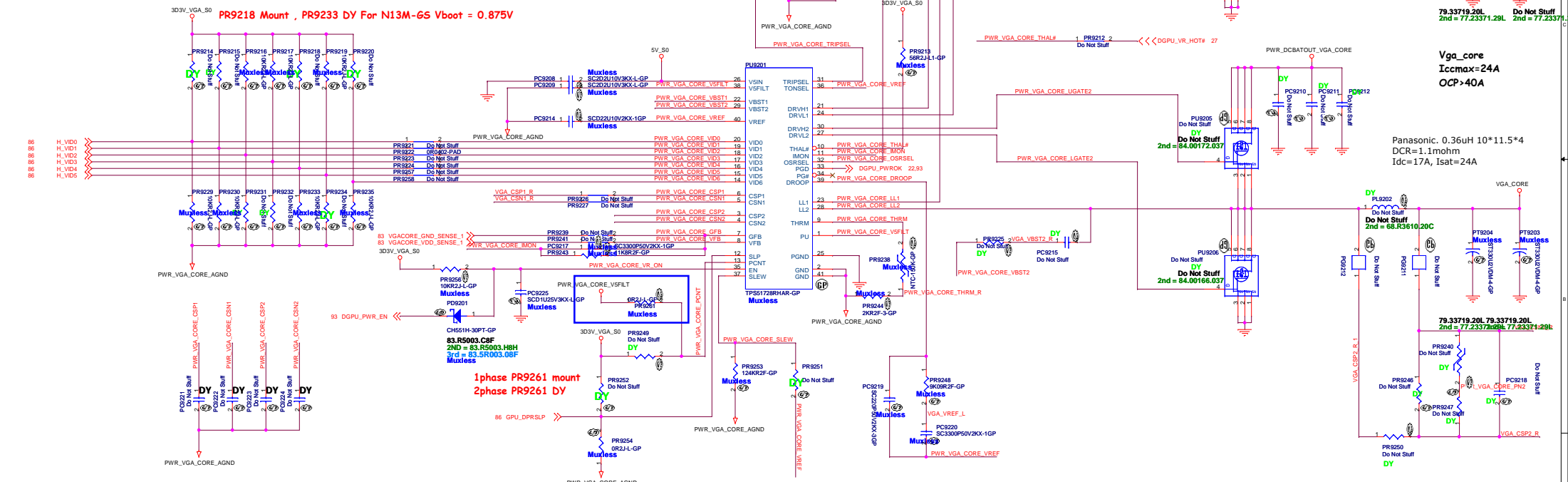
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size Custom		Document Number	
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GPU-VRAM7,8 (4/4)		Rev -4M	
Husk/Petra		-4M	

SSID = PWR.Plane.Regulator_GFX

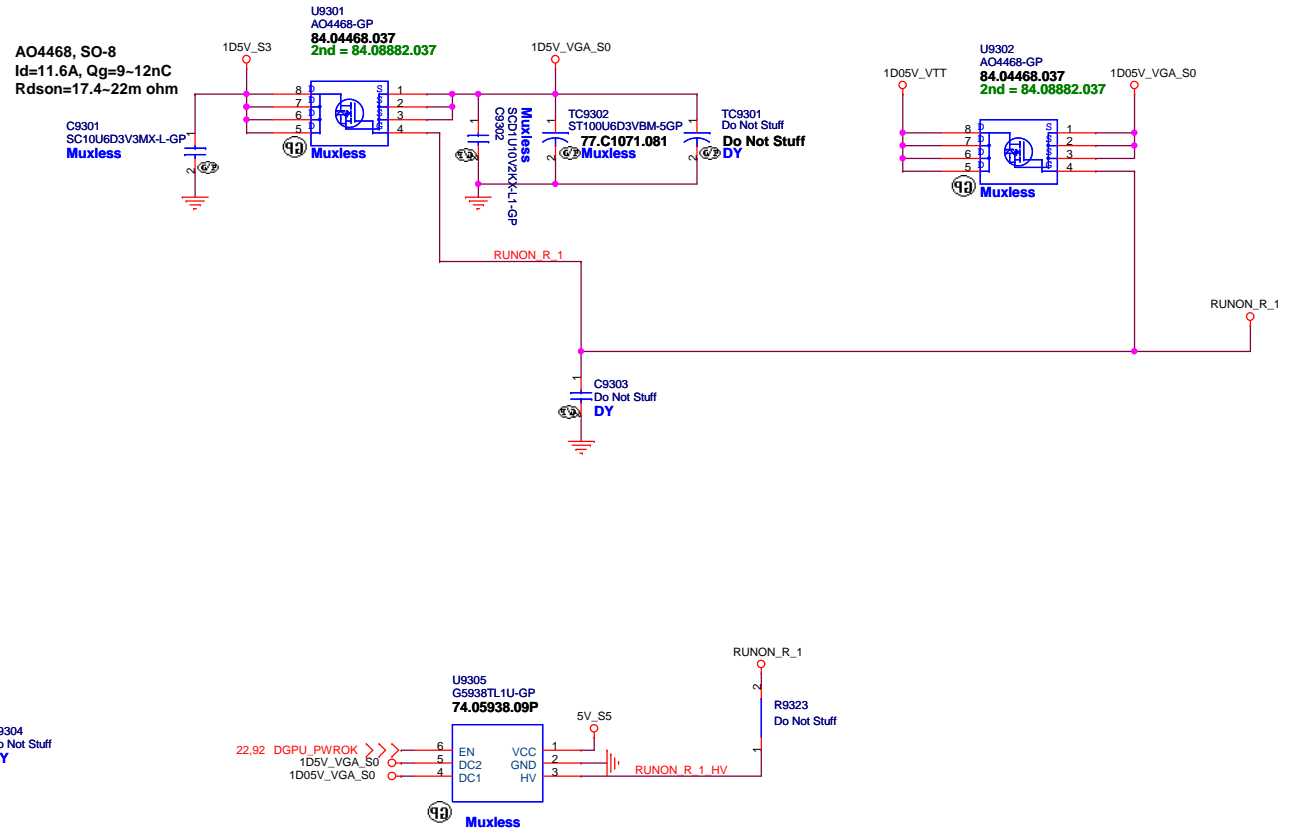
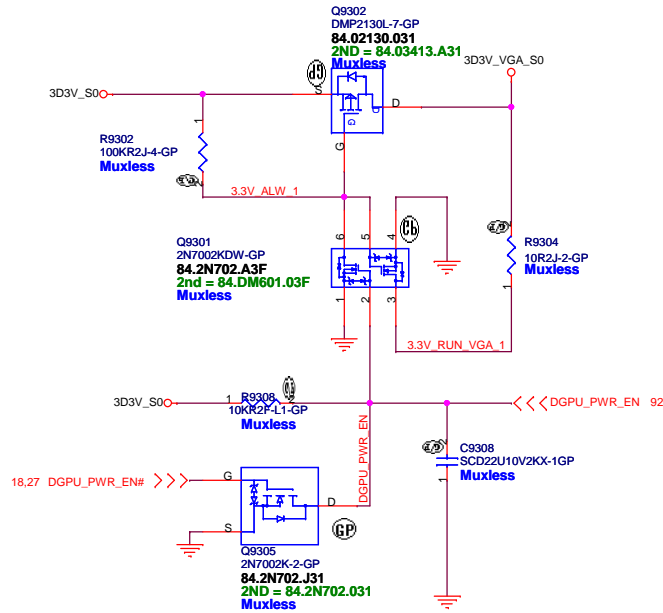


	N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.80U	N13M-GS 71.0N13M.E0U
NV_VDD Boot Voltage	0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215 DY	DY	63.10334.L0L
	PR9230 63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217 DY	63.10334.L0L	DY
	PR9232 63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218 63.10334.L0L	DY	63.10334.L0L
	PR9233 DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V



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DIS I/B Touch

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Title			
DISCRETE VGA POWER			
Size	Document Number	Rev	
Custom	Husk/Petra	-4M	
Date:	Thursday, September 06, 2012	Sheet	93 of 103

5

4

3

2

1

D

D

C

C

B

B

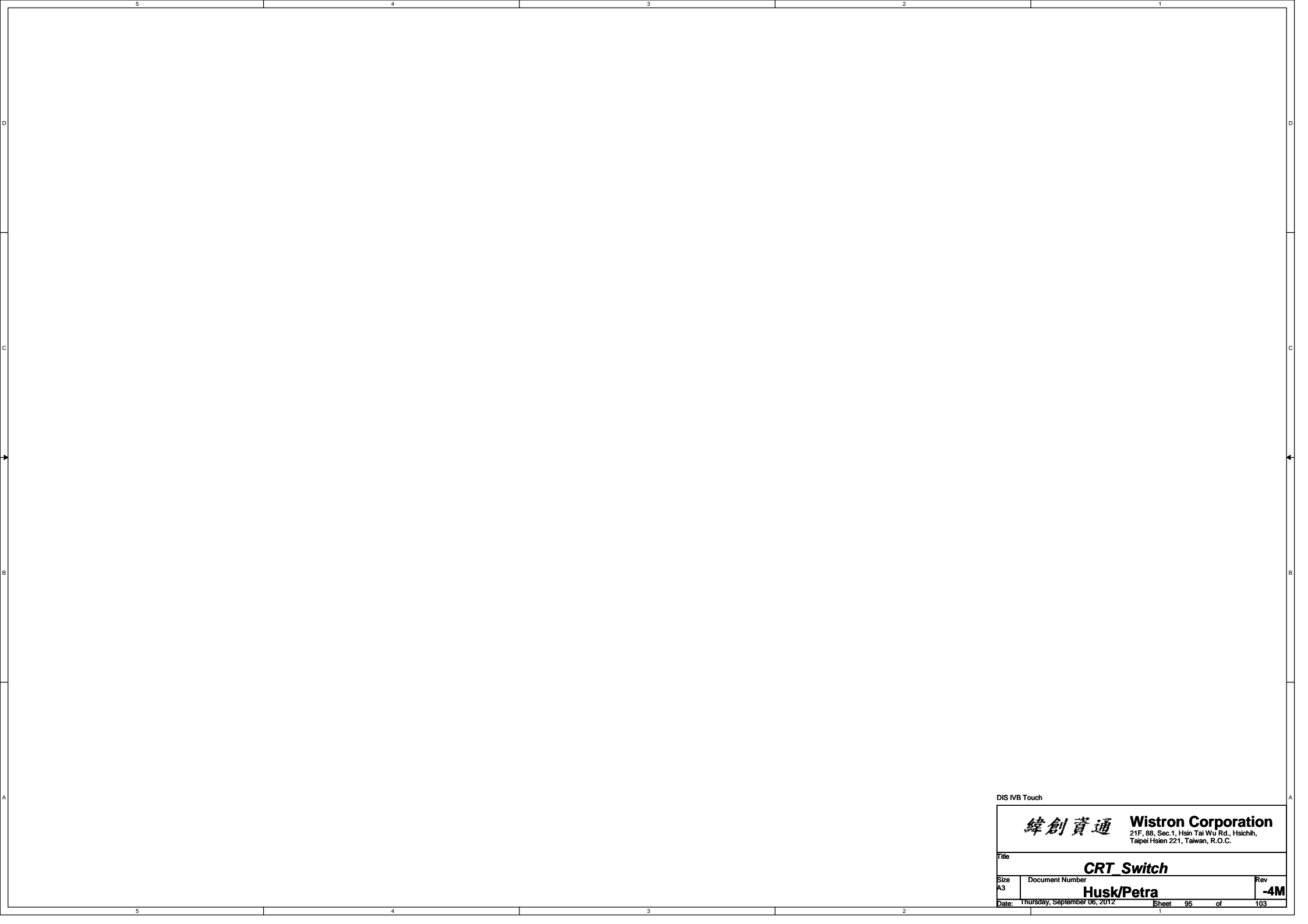
A

A

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DIS IVB Touch

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Title <div>LVDS Switch</div>		
Size <div>A4</div>	Document Number <div>Husk/Petra</div>	Rev <div>-4M</div>
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D

D

C

C

B

B

A

A

DIS IVB Touch

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Title			
CRT Switch			
Size	Document Number		Rev
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5

4

3

2

1

SSID = SDIO

DIS I/B Touch

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size
A2

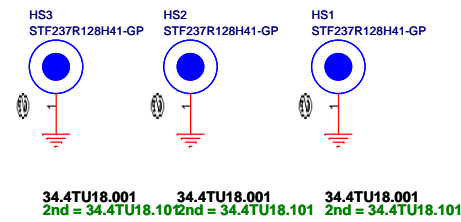
Document Number
Husk/Petra

Rev
-4M

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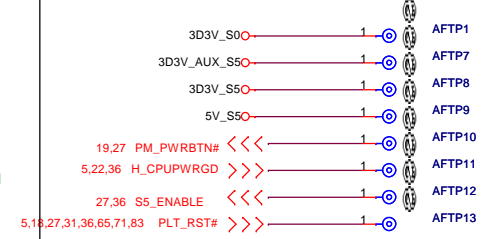
CPU



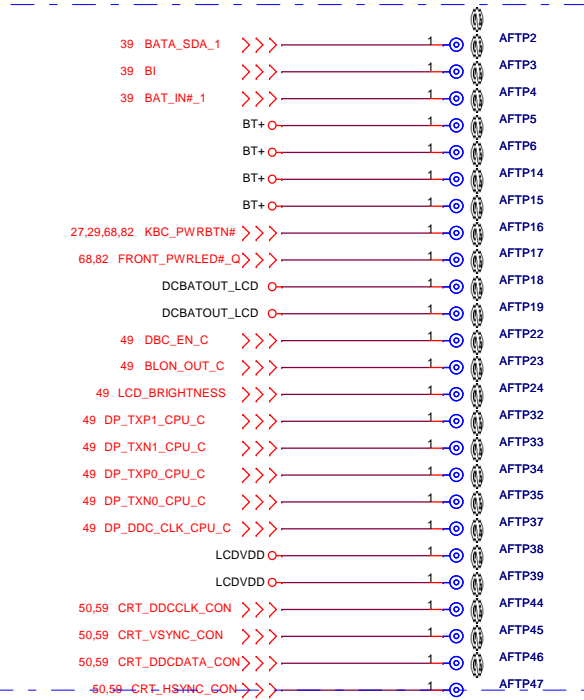
VGA



Check test point

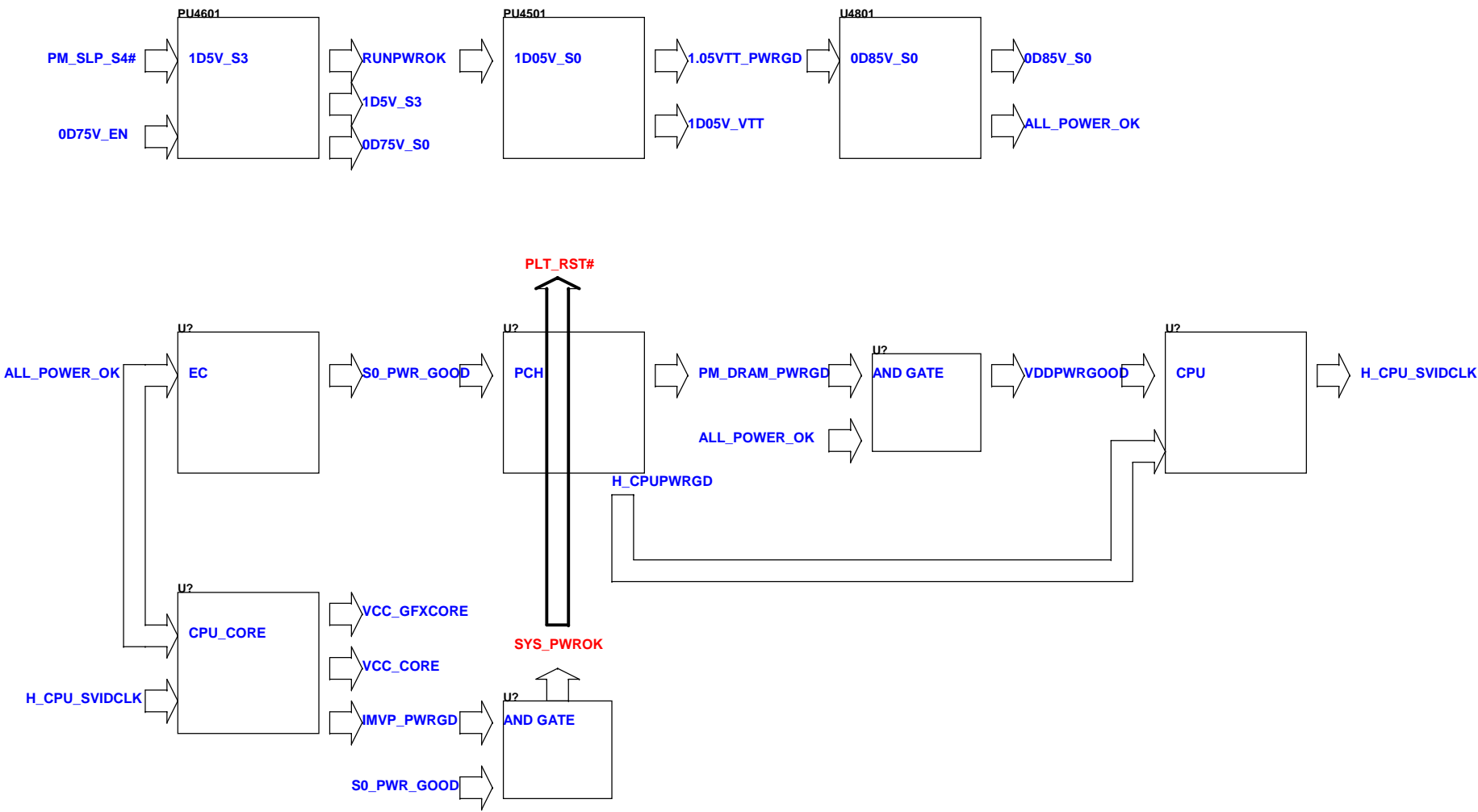


Test Point放在Dimm Door打開可量測處



-4M-201208031615

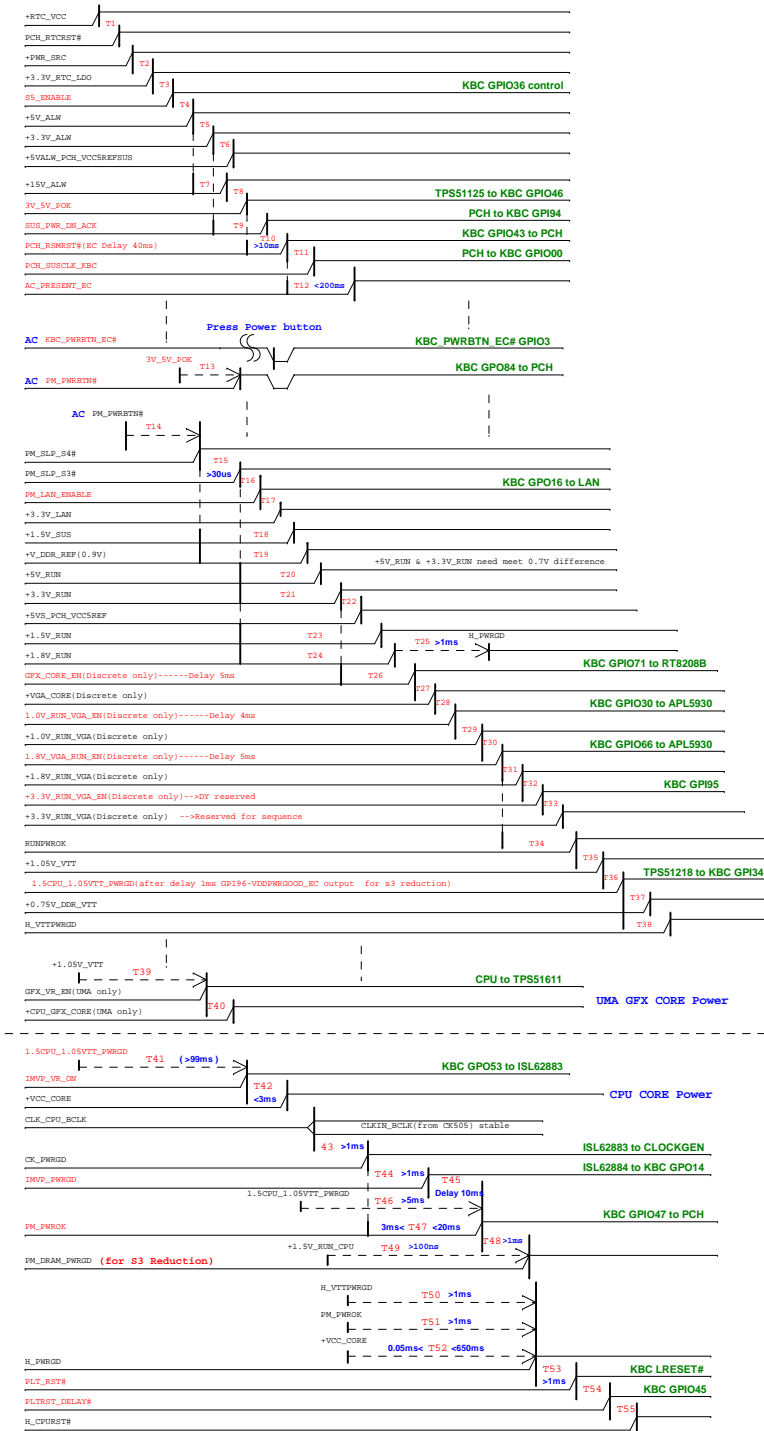
Power Sequence



Intel-Power Up Sequence

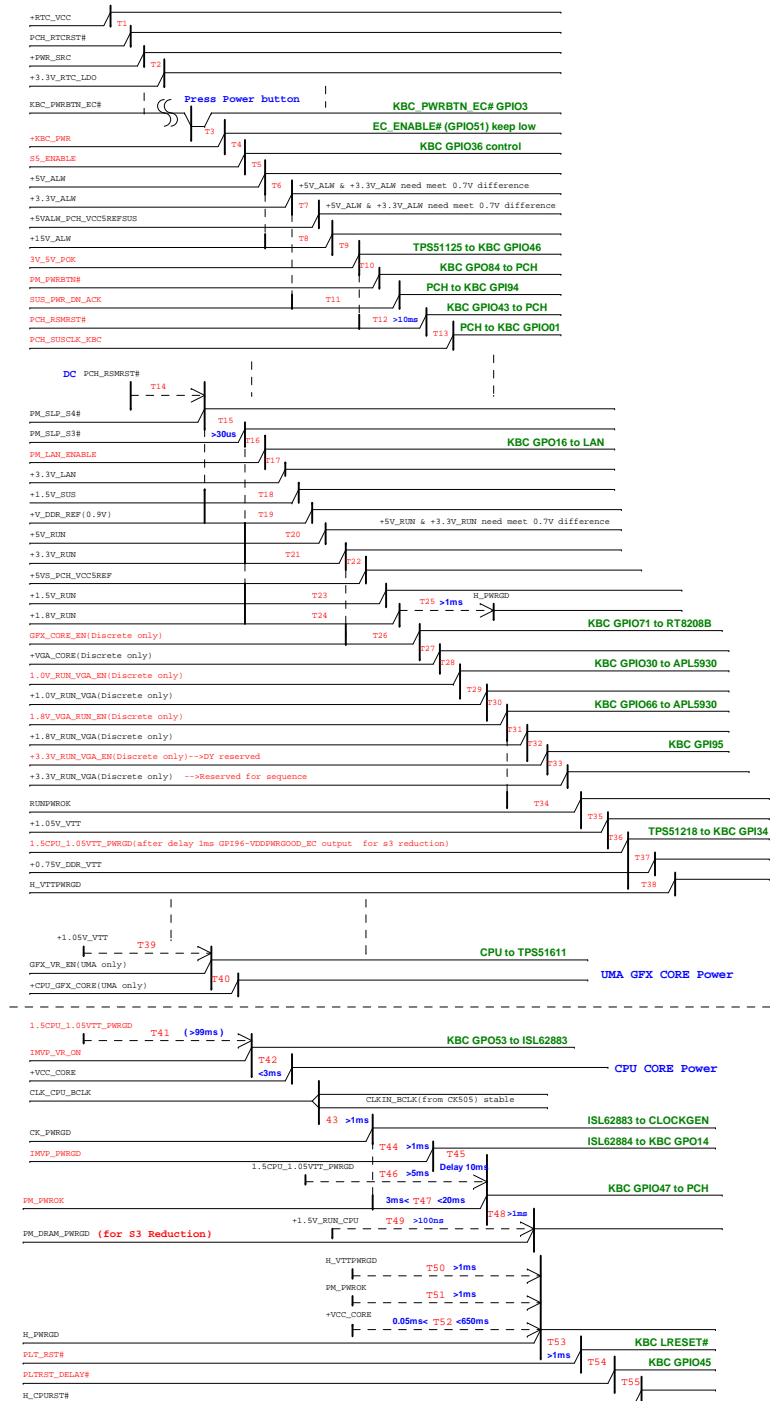
(AC mode)

red word: KBC GPIO

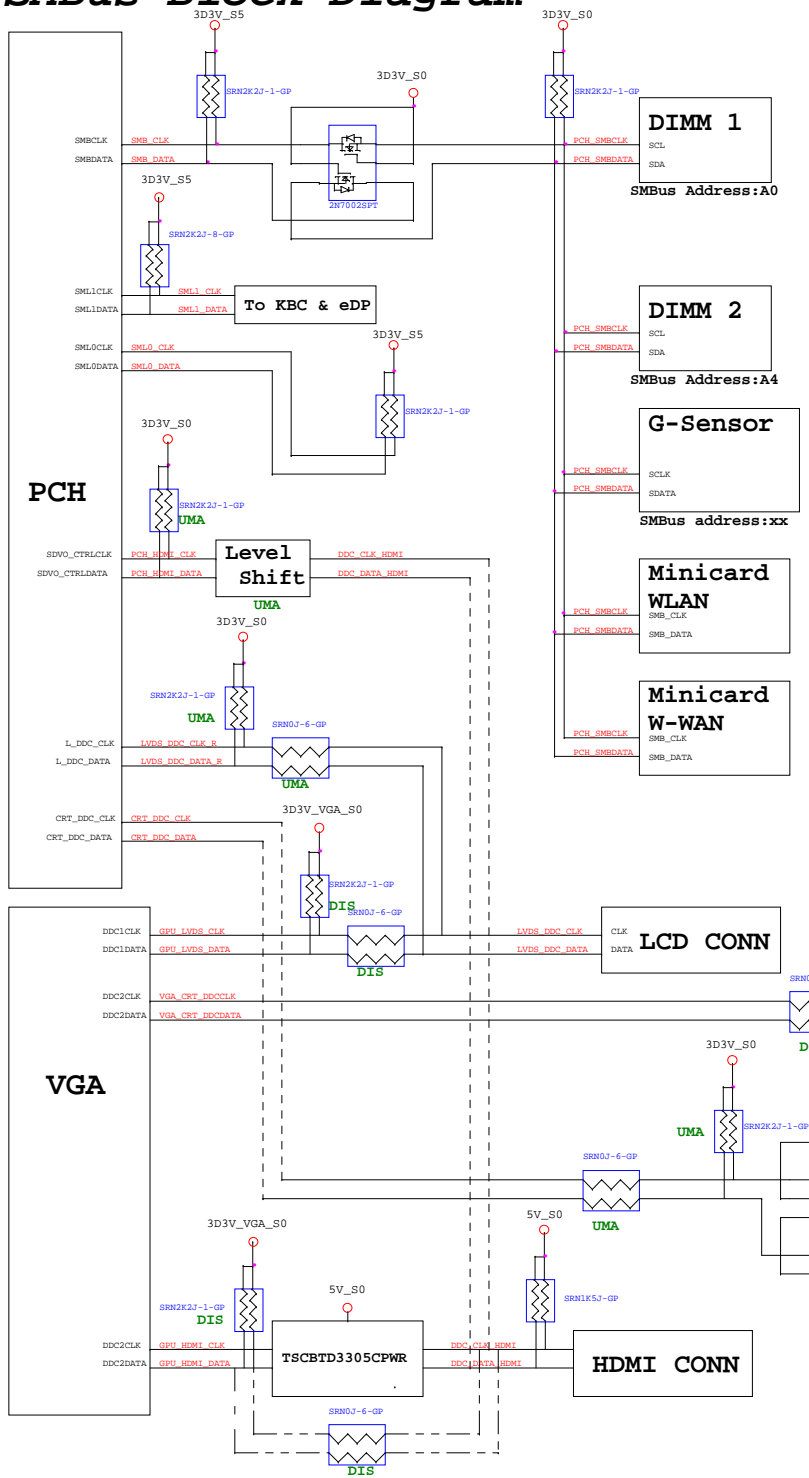


(DC mode)

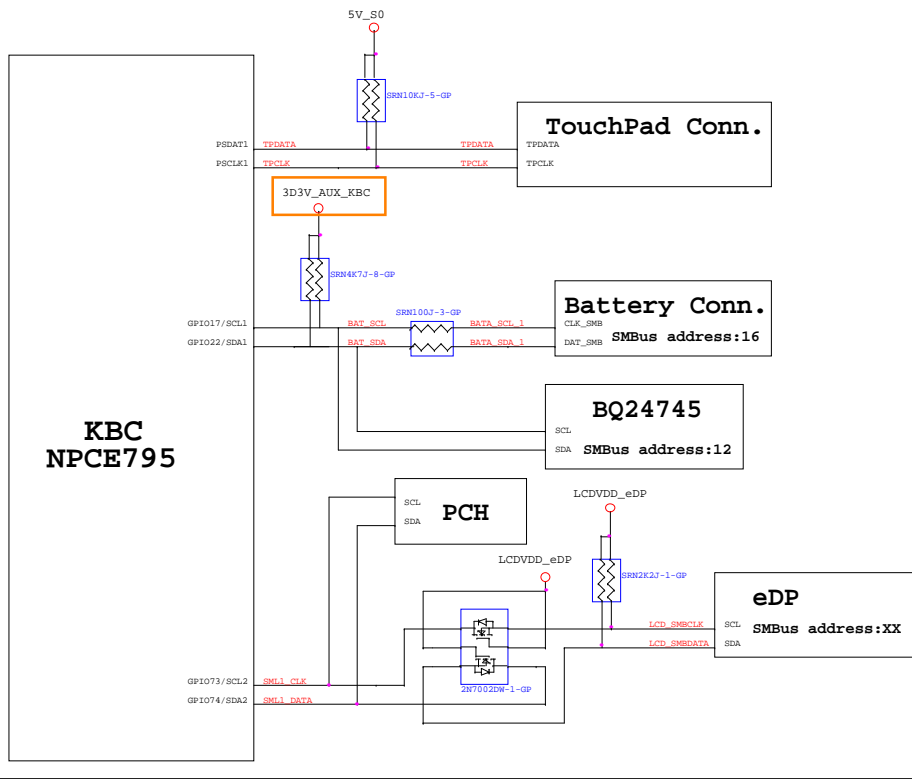
red word: KBC GPIO



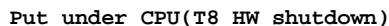
PCH SMBus Block Diagram



KBC SMBus Block Diagram



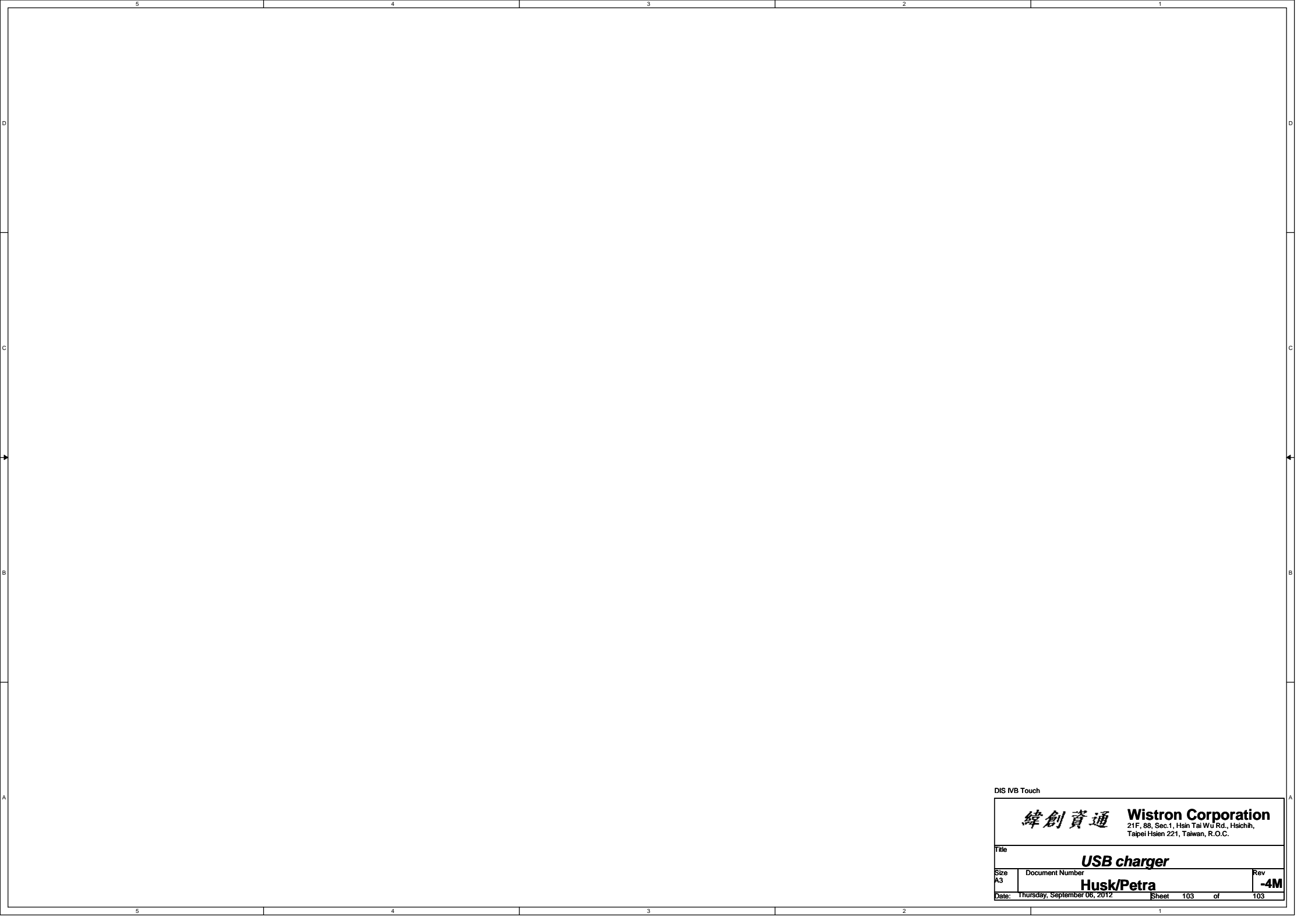
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Codec
ALC271



Title Thermal/Audio Block Diagram			
Size Custom	Document Number Husk/Petra		Rev -4M
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Title			
USB charger			
Size	Document Number		Rev
A3	Husk/Petra		-4M
Date:	Thursday, September 06, 2012	Sheet	103 of 103